ATCA-7368

Installation and Use

P/N: 6806800M12E

September 2015

ARTESYN™

EMBEDDED TECHNOLOGIES

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Safety Notes

This section provides warnings that precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed during all phases of operation, service, and repair of this equipment. You should also employ all other safety precautions necessary for the operation of the equipment in your operating environment. Failure to comply with these precautions or with specific warnings elsewhere in this manual could result in personal injury or damage to the equipment.

Artesyn Embedded Technologies intends to provide all necessary information to install and handle the product in this manual. Because of the complexity of this product and its various uses, we do not guarantee that the given information is complete. If you need additional information, ask your Artesyn representative.

The product has been designed to meet the standard industrial safety requirements. It must not be used except in its specific area of office telecommunication industry and industrial control.

Only personnel trained by Artesyn or persons qualified in electronics or electrical engineering are authorized to install, remove or maintain the product.

The information given in this manual is meant to complete the knowledge of a specialist and must not be used as replacement for qualified personnel.

Keep away from live circuits inside the equipment. Operating personnel must not remove equipment covers. Only factory authorized service personnel or other qualified service personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment.

Do not install substitute parts or perform any unauthorized modification of the equipment or the warranty may be voided. Contact your local Artesyn representative for service and repair to make sure that all safety features are maintained.

EMC

The blade has been tested in a standard Artesyn system and found to comply with the limits for a Class A digital device in this system, pursuant to part 15 of the FCC Rules, EN 55022 Class A respectively. These limits are designed to provide reasonable protection against harmful interference when the system is operated in a commercial environment.

This is a Class A product based on the standard of the Voluntary Control Council for Interference by Information Technology Interference (VCCI). If this equipment is used in a domestic environment, radio disturbance may arise. When such trouble occurs, the user may be required to take corrective actions.

The blade generates and uses radio frequency energy and, if not installed properly and used in accordance with this guide, may cause harmful interference to radio communications. Operating the system in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his own expense.

Installation

Damage of Circuits
Electrostatic discharge and incorrect blade installation and removal can damage circuits or shorten their life.
Before touching the blade or electronic components, make sure that you are working in an ESD-safe environment.

Data Loss
Removing the blade with the blue LED still blinking causes data loss.
Wait until the blue LED is permanently illuminated, before removing the blade.

Damage of Blade and Additional Devices and Modules
Incorrect installation of additional devices or modules may damage the blade or the additional devices or modules.
Before installing or removing an additional device or module, read the respective documentation

System Damage
WARNING: The intra-building port (s) of the equipment or subassembly is suitable for connection to intra-building or unexposed wiring or cabling only. The intra-building port (s) of the equipment or subassembly MUST NOT be metallically connected to interfaces that connect to the outside plant (OSP) or its wiring. These interfaces are designed for use as intra-building interfaces only (Type 2 or Type 4 ports as described in GR-1089) and require isolation from the exposed OSP cabling. The addition of primary protectors is not sufficient protection

in order to connect these interfaces metallically to OSP wiring.
The intra-building port(s) of the equipment or subassembly must use shielded intra-building cabling/wiring that is grounded at both ends.

Operation

Blade Damage
Blade surface
High humidity and condensation on the blade surface causes short circuits.
Do not operate the blade outside the specified environmental limits. Make sure the blade is completely dry and there is no moisture on any surface before applying power.

Blade Overheating and Blade Damage
Operating the blade without forced air cooling may lead to blade overheating and thus blade damage.
When operating the blade, make sure that forced air cooling is available in the shelf.

When operating the blade in areas of electromagnetic radiation ensure that the blade is bolted on the system and the system is shielded by enclosure.

Injuries or Short Circuits
Blade or power supply
In case the ORing diodes of the blade fail, the blade may trigger a short circuit between input line A and input line B so that line A remains powered even if it is disconnected from the power supply circuit (and vice versa).
To avoid damage or injuries, always check that there is no more voltage on the line that has been disconnected before continuing your work.

Switch Settings

Blade Malfunction
Switches marked as 'reserved' might carry production-related functions and can cause the blade to malfunction if their setting is changed.
Therefore, do not change settings of switches marked as 'reserved'. The setting of switches which are not marked as 'reserved' has to be checked and changed before blade installation.

Blade Damage
Setting/resetting the switches during operation can cause blade damage.
Therefore, check and change switch settings before you install the blade.

Battery

Blade Damage
Wrong battery installation may result in hazardous explosion and blade damage.
Therefore, always use the same type of Lithium battery as is installed and make sure the battery is installed as described in this manual.

Environment

Always dispose of used blades, system components and RTMs according to your country's legislation and manufacturer's instructions.

Sicherheitshinweise

Dieses Kapitel enthält Hinweise, die potentiell gefährlichen Prozeduren innerhalb dieses Handbuchs vorrangestellt sind. Beachten Sie unbedingt in allen Phasen des Betriebs, der Wartung und der Reparatur des Systems die Anweisungen, die diesen Hinweisen enthalten sind. Sie sollten außerdem alle anderen Vorsichtsmaßnahmen treffen, die für den Betrieb des Produktes innerhalb Ihrer Betriebsumgebung notwendig sind. Wenn Sie diese Vorsichtsmaßnahmen oder Sicherheitshinweise, die an anderer Stelle diese Handbuchs enthalten sind, nicht beachten, kann das Verletzungen oder Schäden am Produkt zur Folge haben.

Artesyn Embedded Technologies ist darauf bedacht, alle notwendigen Informationen zum Einbau und zum Umgang mit dem Produkt in diesem Handbuch bereit zu stellen. Da es sich jedoch um ein komplexes Produkt mit vielfältigen Einsatzmöglichkeiten handelt, können wir die Vollständigkeit der im Handbuch enthaltenen Informationen nicht garantieren. Falls Sie weitere Informationen benötigen sollten, wenden Sie sich bitte an die für Sie zuständige Geschäftsstelle von Artesyn.

Das System erfüllt die für die Industrie geforderten Sicherheitsvorschriften und darf ausschließlich für Anwendungen in der Telekommunikationsindustrie und im Zusammenhang mit Industriesteuerungen verwendet werden.

Einbau, Wartung und Betrieb dürfen nur von durch Artesyn ausgebildetem oder im Bereich Elektronik oder Elektrotechnik qualifiziertem Personal durchgeführt werden. Die in diesem Handbuch enthaltenen Informationen dienen ausschließlich dazu, das Wissen von Fachpersonal zu ergänzen, können dieses jedoch nicht ersetzen.

Halten Sie sich von stromführenden Leitungen innerhalb des Produktes fern. Entfernen Sie auf keinen Fall Abdeckungen am Produkt. Nur werksseitig zugelassenes Wartungspersonal oder anderweitig qualifiziertes Wartungspersonal darf Abdeckungen entfernen, um Komponenten zu ersetzen oder andere Anpassungen vorzunehmen.

Installieren Sie keine Ersatzteile oder führen Sie keine unerlaubten Veränderungen am Produkt durch, sonst verfällt die Garantie. Wenden Sie sich für Wartung oder Reparatur bitte an die für Sie zuständige Geschäftsstelle von Artesyn. So stellen Sie sicher, dass alle sicherheitsrelevanten Aspekte beachtet werden.

EMV

Das Blade wurde in einem Artesyn Standardsystem getestet. Es erfüllt die für digitale Geräte der Klasse A gültigen Grenzwerte in einem solchen System gemäß den FCC-Richtlinien Abschnitt 15 bzw. EN 55022 Klasse A. Diese Grenzwerte sollen einen angemessenen Schutz vor Störstrahlung beim Betrieb des Blades in Gewerbe- sowie Industriegebieten gewährleisten.

Das Blade arbeitet im Hochfrequenzbereich und erzeugt Störstrahlung. Bei unsachgemäßem Einbau und anderem als in diesem Handbuch beschriebenen Betrieb können Störungen im Hochfrequenzbereich auftreten.

Warnung! Dies ist eine Einrichtung der Klasse A. Diese Einrichtung kann im Wohnbereich Funkstörungen verursachen. In diesem Fall kann vom Betreiber verlangt werden, angemessene Maßnahmen durchzuführen.

Installation

Beschädigung von Schaltkreisen
Elektrostatische Entladung und unsachgemäßer Ein- und Ausbau von Blades kann Schaltkreise beschädigen oder ihre Lebensdauer verkürzen.
Bevor Sie Blades oder elektronische Komponenten berühren, vergewissern Sie sich, daß Sie in einem ESD-geschützten Bereich arbeiten.

Datenverlust
Wenn Sie das Blade aus dem Shelf herausziehen, und die blaue LED blinkt noch, gehen Daten verloren.
Warten Sie bis die blaue LED durchgehend leuchtet, bevor Sie das Blade herausziehen.

Beschädigung des Blades und von Zusatzmodulen
Fehlerhafte Installation von Zusatzmodulen, kann zur Beschädigung des Blades und der Zusatzmodule führen.
Lesen Sie daher vor der Installation von Zusatzmodulen die zugehörige Dokumentation.

Beschädigung des Systems
Warnung: Die intra-Gebäude Port (s) des Geräts oder Baugruppe ist für den Anschluss an den inner Gebäude oder unbelichteten Verdrahtung oder Verkabelung nur. Die intra-Gebäude Port(s) des Geräts oder Baugruppe muss nicht metallisch mit Schnittstellen, die an der Außenanlage (OSP) oder dessen Verkabelung anschließen angeschlossen werden. Diese Schnittstellen sind für die Verwendung als intra Gebäude Schnittstellen nur entworfen, (Typ 2 oder Typ 4 Ports wie in GR-1089 beschrieben) und erfordern Isolierung von der freiliegenden OSP-Verkabelung. Die Zugabe von primären Schutz nicht ausreichenden Schutz, um diese Schnittstellen metallisch mit OSP Verdrahtung verbinden.
Die intra-Gebäude Port (s) des Gerätes oder einer Unterbaugruppe müssen abgeschirmte innerGebäudeVerkabelung / Verdrahtung, die an beiden Enden geerdet ist zu verwenden.

Betrieb

Beschädigung des Blades
Hohe Luftfeuchtigkeit und Kondensat auf der Oberfläche des Blades können zu Kurzschlüssen führen.
Betreiben Sie das Blade nur innerhalb der angegebenen Grenzwerte für die relative Luftfeuchtigkeit und Temperatur. Stellen Sie vor dem Einschalten des Stroms sicher, dass sich auf dem Blade kein Kondensat befindet.

Überhitzung und Beschädigung des Blades
Betreiben Sie das Blade ohne Zwangsbelüftung, kann das Blade überhitzt und schließlich beschädigt werden.
Bevor Sie das Blade betreiben, müssen Sie sicher stellen, dass das Shelf über eine Zwangskühlung verfügt.

Wenn Sie das Blade in Gebieten mit starker elektromagnetischer Strahlung betreiben, stellen Sie sicher, dass das Blade mit dem System verschraubt ist und das System durch ein Gehäuse abgeschirmt wird.

Verletzungen oder Kurzschlüsse
Blade oder Stromversorgung

Falls die ORing Dioden des Blades durchbrennen, kann das Blade einen Kurzschluss zwischen den Eingangsleitungen A und B verursachen. In diesem Fall ist Leitung A immer noch unter Spannung, auch wenn sie vom Versorgungskreislauf getrennt ist (und umgekehrt).
Prüfen Sie deshalb immer, ob die Leitung spannungsfrei ist, bevor Sie Ihre Arbeit fortsetzen, um Schäden oder Verletzungen zu vermeiden.

Schaltereinstellungen

Fehlfunktion des Blades
Schalter, die mit 'Reserved' gekennzeichnet sind, können mit produktionsrelevanten Funktionen belegt sein. Das Ändern dieser Schalter kann im normalen Betrieb Störungen auslösen.
Verstellen Sie nur solche Schalter, die nicht mit 'Reserved' gekennzeichnet sind. Prüfen und ändern Sie die Einstellungen der nicht mit 'Reserved' gekennzeichneten Schalter, bevor Sie das Blade installieren.

Beschädigung der Blade
Das Verstellen von Schaltern während des laufenden Betriebes kann zur Beschädigung des Blades führen.
Prüfen und ändern Sie die Schaltereinstellungen, bevor Sie das Blade installieren.

Batterie

Beschädigung des Blades
Ein unsachgemäßer Einbau der Batterie kann gefährliche Explosionen und Beschädigungen des Blades zur Folge haben.
Verwenden Sie deshalb nur den Batterietyp, der auch bereits eingesetzt wurde und befolgen Sie die Installationsanleitung.

Umweltschutz

Entsorgen Sie alte Batterien und/oder Blades/Systemkomponenten/RTMs stets gemäß der in Ihrem Land gültigen Gesetzgebung und den Empfehlungen des Herstellers.

About this Manual

Overview of Contents

This manual is intended for users qualified in electronics or electrical engineering. Users must have a working understanding of Peripheral Component Interconnect (PCI), AdvancedTCA®, and telecommunications.

The manual contains the following chapters and appendices:

- *About this Manual* on page 23 lists all conventions and abbreviations used in this manual and outlines the revision history.
- *Safety Notes* on page 15 lists safety notes applicable to the blade.
- *Sicherheitshinweise* on page 19 provides the German translation of the safety notes section.
- *Introduction* on page 31 describes the main features of the blade.
- *Hardware Preparation and Installation* on page 41 outlines the installation requirements, hardware accessories, switch settings, installation and removal procedures.
- *Controls, Indicators, and Connectors* on page 59 describes external interfaces of the blade. This includes connectors and LEDs.
- *BIOS* on page 67 describes the features and setup of BIOS.
- *Functional Description* on page 85 describes the functional blocks of the blade in detail. This includes a block diagram, description of the main components used and so on.
- *Serial Over LAN* on page 97 provides information on how to establish a serial-over LAN session on your blade.
- *Supported IPMI Commands* on page 103 lists all supported IPMI commands.
- *FRU Information and SDR Summary* on page 147 provides information on the blade's FRU information and sensor data.
- *Replacing the Battery* on page 215 provides the procedures in changing the battery.
- *Related Documentation* on page 219 provides links to further blade-related documentation.

Abbreviations

This document uses the following abbreviations:

Abbreviation	Definition
AMC	Advanced Mezzanine Card
AMC.x	A generic reference to all AMC specifications (AMC.0, AMC.1, AMC.2, AMC.3)
AMC Bay	A single AMC site on an AMC carrier
ATCA	Advanced Telecommunications Computing Architecture
AVR	Atmel's 8-bit RISC micro-controller family
BBS	Basic Blade Services
BGA	Ball Grid Array
BIOS	Basic Input/Output System
BOM	Bill of Material
CFM	Cubic Feet per Minute
CG	Carrier-grade
CK409B	Clock generator standard for Intel chipset platforms
CPLD	Complex Programmable Logic Device
CPM	Critical Parameter Management
DDR	Dual Data Rate (type of SDRAM)
DDR3	Double Data Rate 3 synchronous dynamic random access memory (SDRAM) is the name of the new DDR memory standard that is being developed as the successor to DDR2 SDRAM.
DFM	Design for Manufacturability
DFT	Design for Test
DMA	Direct Memory Access
DRAM	Dynamic Random Access Memory
ECC	Error Correction Code
EMC	Electro-magnetic Compatibility

Abbreviation	Definition
EMI	Electro-magnetic Interference
ESD	Electro-static Discharge
FMECA	Failure Mode, Effects and Criticality Analysis
FRU	Field Replaceable Unit
FSB	Front-side Bus
FWH	Firmware Hub
GA	General Availability
Gb	Gigabit(s)
Gbps	Gigabits per second
GHz	Gigahertz
GigE	Gigabit Ethernet
GPIO	General Purpose Input/Output
I2C	Inter Integrated-Circuit Bus (2-wire serial bus and protocol)
I/O	Input/Output
IA-32	32-bit Intel processor architecture
ICH	I/O Control Hub (also called "South Bridge")
ICT	In-circuit Test
IMC	Integrated Memory Controller
IPMB	Intelligent Platform Management Bus
IPMB-L	The IPMB connecting the carrier IPMC to the AMC module
Intel® QuickPath Interconnect (Intel® QPI)	A cache-coherent, link-based Interconnect specification for Intel processors, chipsets, and I/O bridge components.
MMC	Intelligent Platform Management Controller
IPMI	Intelligent Platform Management Interface
ITP	In-Target Probe
ITP700	An ITP scheme defined by Intel
JTAG	Joint Test Action Group (test interface for digital logic circuits)
L2	Level 2 (as in "L2 Cache")

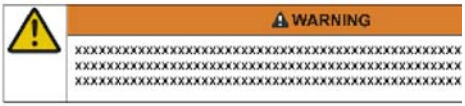
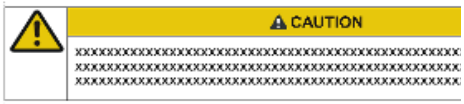
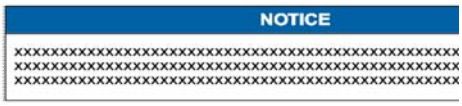
Abbreviation	Definition
LFM	Linear Feet per Minute
LPC	Low Pin Count
LVDS	Low Voltage Differential Signaling
MAC	Medium Access Controller
Mb(ps)	Megabits (per second)
MB(ps)	Megabytes (per second)
MCH	Memory Controller Hub (also called "North Bridge")
MHz	Megahertz
MMC	Module Management Controller
Module	This term is used to refer to the Module card in this document
MP	Management Power
MTBF	Mean Time Between Failures
MTTR	Mean Time To Repair
N/A	Not Applicable
NEBS	Network Equipment Building System
NMI	Non-maskable Interrupt
NT	Non-transparent
NVRAM	Non-volatile Random Access Memory
OEM	Original Equipment Manufacturer
OOS	Out-of-service
PCB	Printed Circuit Board
PCI-E	PCI-Express
PHY	Physical layer device (for ethernet)
PICMG	PCI Industrial Computer Manufacturers Group
PLL	Phase Locked Loop
POST	Power-on Self Test
PP	Payload Power
PRD	Product Requirements Document

Abbreviation	Definition
RC	Root Complex
RoHS	Restriction of Hazardous Substances
RS232	Recommended Standard 232C - interface standard for serial communication
RTC	Real-Time Clock
Rx	Receive line (of a duplex serial communication interface)
SATA	Serial AT Attachment (high-speed serial interface standard for storage devices)
SDR	Sensor Data Record
SDRAM	Synchronous Dynamic Random Access Memory
SELV	Safety Extra Low Voltage
SerDes	Serializer-Deserializer
SIMD	Single Instruction Multiple Data
SMBus	System Management Bus
SMI	System Management Interrupt
SODIMM	Small Outline Dual-in-line Memory Module
SPD	Serial Presence Detect
TBD	To be decided
TCP	Transmission Control Protocol
TDP	Thermal Design Power
Tx	Transmit line (of a duplex serial communication interface)
UART	Universal Asynchronous Receiver-Transmitter
UDP	User Datagram Protocol
VID	Voltage Identification (for Intel CPUs)
Westmere	Intel Codename for next gen.(after Core2Duo) Intel CPU microarchitecture
Tylersburg	Intel Codename for Intel IOH36D device
Zoar	Intel Codename for Intel 82576 Ethernet device

Conventions

The following table describes the conventions used throughout this manual.

Notation	Description
0x00000000	Typical notation for hexadecimal numbers (digits are 0 through F), for example used for addresses and offsets
0b0000	Same for binary numbers (digits are 0 and 1)
bold	Used to emphasize a word
`Screen`	Used for on-screen output and code related elements or commands in body text
`Courier + Bold`	Used to characterize user input and to separate it from system output
Reference	Used for references and for table and figure descriptions
File > Exit	Notation for selecting a submenu
<text>	Notation for variables and keys
[text]	Notation for software buttons to click on the screen and parameter description
...	Repeated item for example node 1, node 2, ..., node 12
. . .	Omission of information from example/command that is not necessary at the time being
..	Ranges, for example: 0..4 means one of the integers 0,1,2,3, and 4 (used in registers)
|	Logical OR

Notation	Description
	Indicates a hazardous situation which, if not avoided, could result in death or serious injury
	Indicates a hazardous situation which, if not avoided, may result in minor or moderate injury
	Indicates a property damage message
	No danger encountered. Pay attention to important information

Summary of Changes

Part Number	Publication Date	Description
6806800M12E	September 2015	Updated the sections *Installation* on page 16 and *Installation* on page 20.
6806800M12D	June 2014	Rebranded to Artesyn.
6806800M12C	February 2014	Updated Table 8-33 on page 193 and Table 8-34 on page 194. Updated Table "Environmental Requirements" on page 43. Updated *Get Handle Switch Command* on page 136 and *Set Handle Switch Command* on page 137.
6806800M12B	January 2012	Final version. Added *Declaration of Conformity* on page 34. Updated Chapter 1, *Mechanical Data, on page 35*. Updated Chapter 2, *Environmental and Power Requirements, on page 42*, Table "Power Requirements" on page 45, and Figure "Blade Layout" on page 46. Updated Chapter 4, *Overview, on page 67*. Updated Table "Ethernet Controller Types" on page 91, Table "Power Configuration" on page 149, Table "-48V A Volts" on page 157, Table "-48V B Volts" on page 158, Table "Inlet Temp" on page 164, Table "Outlet Temp" on page 167, and Table "CPU Temp" on page 171.
6806800M12A	March 2011	EA version

1.1 Features

ATCA-7368 is a high performance single processor AdvancedTCA Server blade and Node board, designed according to PICMG 3.0 Revision 3.0 Advanced TCA Base Specification. The ATCA-7368 is a single board computer that offers a powerful processing complex through a single six-core Intel Westmere-EP processor, and support for up to 48GB DDR3 memory. Furthermore ATCA-7368 provides local storage (Onboard SATA disk/SATA Cube, onboard flash disk, or through the RTM), standard I/O and redundant Gigabit Ethernet connections to the back plane's Base Interfaces (PICMG3.0) and Fabric Interfaces (PICMG 3.1 Option1,9). Another important feature is that ATCA-7368 provides AMC support and is compatible with different AMC boards to meet application-specific requirements. The ATCA-7368 provides system management capabilities and is hot swap compatible based on the ATCA specification.

The following lists the main features of ATCA-7368:

- Form factor: Single slot ATCA (280mm x 322mm)
- Processor: Intel Westmere-EP Six-Core processor (Intel Xeon 5600 series), Drop-in compatible with Intel Nehalem-EP processor (Intel Xeon 5500 Series)
- North Bridge: Xeon 5520 (Tylersburg IOH36 D)
  - Provides two QPI interfaces for connecting to up to two Intel Xeon processors
  - Provides 36 PCI-e Gen2 lanes, Intel Virtualization Technology, ESI interface and Management Engine
  - FC-BGA 37.5mm x 37.5 mm, 1295 balls
- South Bridge: ICH10R, ESI connection to Xeon 5520 (Tylersburg IOH36 D)
  - Provides extensive I/O support and Boot path to redundant SPI Boot flashes
  - I/O interfaces include SATA, USB2.0, LAN, LPC interface, RTC with WDT
- Base interface: Dual 10/100/1000Base-T Ethernet
- Fabric Interface: Dual 1G/10Gbps Ethernet interfaces, support PICMG3.1 option 1 and 9
- Update Channel: One 10/100/1000Base-T, and SAS ports
- RTM Interface
  - One PCI-E x4
  - Dual GbE SFP SerDes and control signal

  - 1x SATA port
  - 1x UART and 1x USB interfaces
  - IPMI Management bus
- One AMC slot
  - PCI-E2.0 x4 on ports 4-7
  - FCLK support
- Front Panel
  - Two 10/100/1000BASE-T Ethernet
  - Two USB2.0 Ports
  - One serial console
- BIOS Chip: Up to 4 MB onboard Boot and 4 MB Recovery Boot Flash (SPI)
- Onboard storage support (optional)
  - SATA Cube (SSD): 16, 32, 64, 128 GB capacity
  - USB flash (EUSB SDD), 1, 2 or 4 GB capacity
- Onboard IPMC (IPMI management controller) implements IPMI version 1.5
- Onboard Glue Logic FPGA for IPMC extension and onboard Control register

1.2 Standard Compliances

The product is designed to meet the following standards.

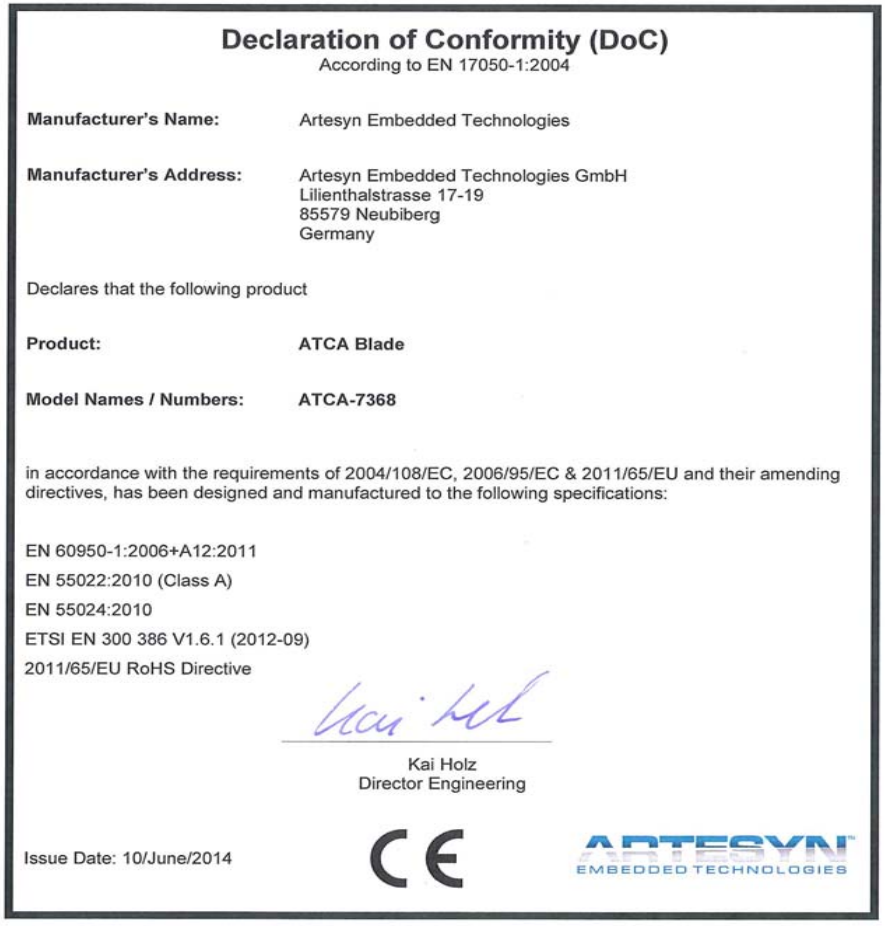
Table 1-1 Standard Compliances

Standard	Description
SN29500/8,	Reliability requirements
MIL-HDBK-217F,	
GR-332,	
TR-NWT-000357	

Table 1-1 Standard Compliances (continued)

Standard	Description
IEC 60068-2-1/2/3/13/14	Climatic environmental requirements. The product can only be used in a restricted temperature range.
IEC 60068-2-27/32/35	Mechanical environmental requirements
EN 60950/UL 60950 (in predefined Force system)	Legal requirements, safety
UL 94V-0/1, Oxygen index for PCBs below 28%	Flammability
EN 55022,	EMC requirements on system level Attention: ATCA boards require CISPR 22 Class B on conducted emissions EMC immunity requirements industrial EMC for telecom equipment
EN 55024,	
EN 61000-6-2,	
EN 300386	
FCC Part 15 Class A	
ANSI/IPC-A-610 Rev.B Class 2,	Manufacturing requirements
ANSI/IPC-R-700B, ANSI-J-001...003	
ISO 8601	Y2K compliance
NEBS Standard GR-63-CORE,	NEBS level three
NEBS Standard GR-1089 CORE	Project is designed to support NEBS level three. The compliance tests must be done with the customer target system.

Figure 1-1 Declaration of Conformity



Declaration of Conformity (DoC)

According to EN 17050-1:2004

Manufacturer's Name: Artesyn Embedded Technologies

Manufacturer's Address: Artesyn Embedded Technologies GmbH
Lilienthalstrasse 17-19
85579 Neubiberg
Germany

Declares that the following product

Product: **ATCA Blade**

Model Names / Numbers: **ATCA-7368**

in accordance with the requirements of 2004/108/EC, 2006/95/EC & 2011/65/EU and their amending directives, has been designed and manufactured to the following specifications:

EN 60950-1:2006+A12:2011
EN 55022:2010 (Class A)
EN 55024:2010
ETSI EN 300 386 V1.6.1 (2012-09)
2011/65/EU RoHS Directive

Kai Holz
Director Engineering

Issue Date: 10/June/2014

CE

ARTESYN EMBEDDED TECHNOLOGIES

1.3 Mechanical Data

The following table provides details about the blade's mechanical data, such as dimensions and weight.

Table 1-2 Mechanical Data

Feature	Value
Dimensions (width x height x depth)	Single slot ATCA 280mm x 322mm
PCBA size	280mm x 322.25mm
Assembly size	351mm x 312mm x 30mm, 8U form factor
Weight of blade with AMC	3053.5g
Weight of blade without AMC and HDD	2862.3g

1.4 Mechanical Layout

The following graphics illustrate the mechanical layout of the blade.

Figure 1-2 Mechanical Layout (with AMC)

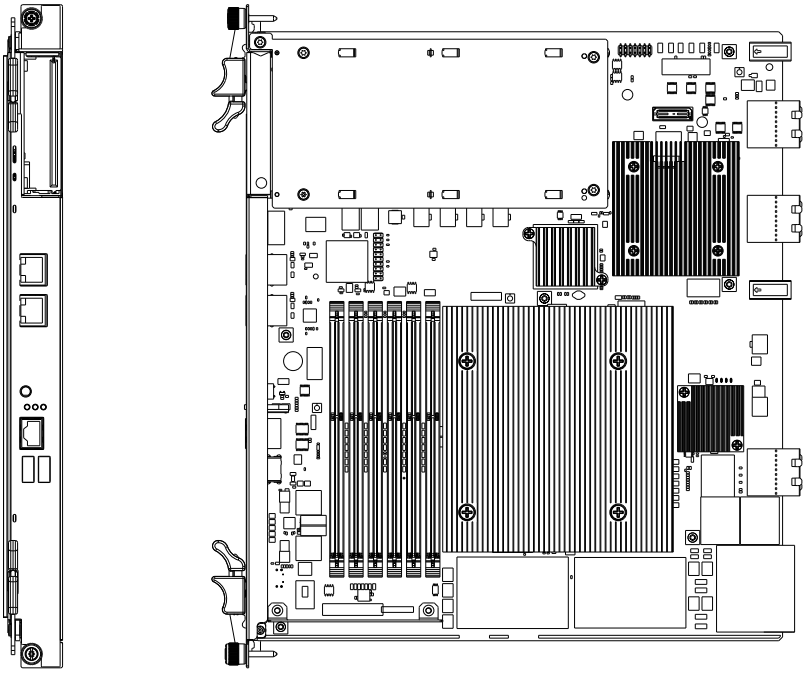


Figure 1-3 Mechanical Layout (without AMC and HDD)

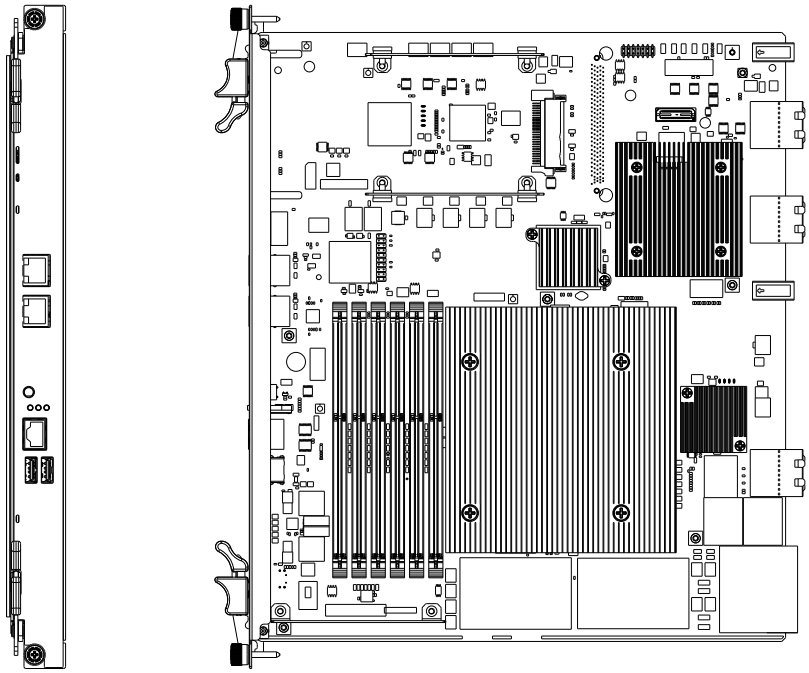
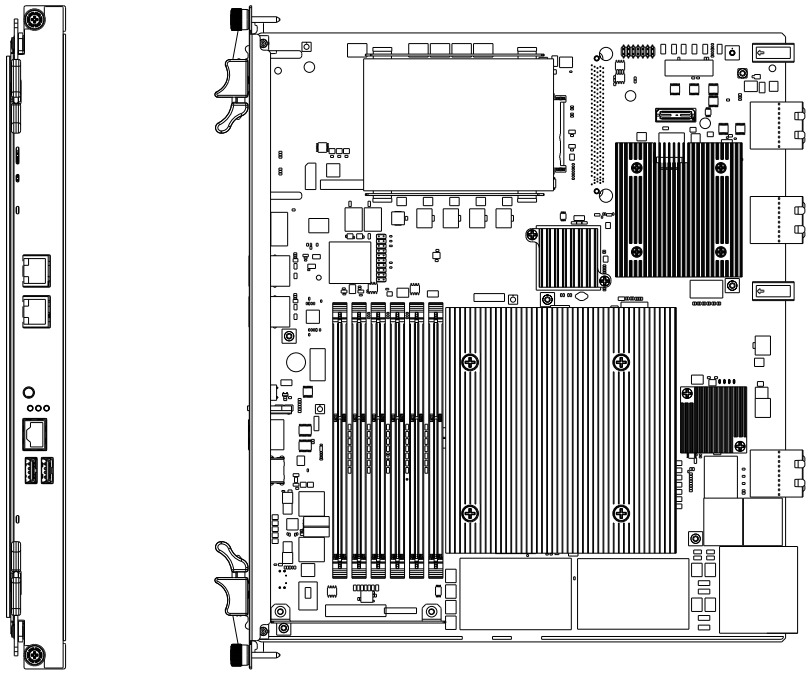


Figure 1-4 Mechanical Layout (without AMC/ with HDD)



1.5 Ordering Information

As of the printing date of this manual, this guide supports the models listed below.

Table 1-3 Blade Variants - Ordering Information

Product Name	Description
ATCA-7368-0GB	ATCA blade, Intel Xeon L5638 6-CORE (2.0 GHZ), 0GB, 10G support, AMC site, no Flash (ROHS 6/6)
ATCA-7368-0GB-LS	ATCA blade, Intel Xeon L5638 6-CORE (2.0 GHZ), 0GB, 10G support, optional onboard hdd, no AMC site, no Flash (ROHS 6/6)
ATCA-7368-0GB-CE	Commercial-ATCA blade, Intel Xeon E5645 6-CORE (2.4 GHZ), 0GB, 10G support, AMC site, no Flash (ROHS 6/6)
ATCA-7368-0GB-LS-CE	Commercial-ATCA blade, Intel Xeon E5645 6-CORE (2.4 GHZ), 0GB, 10G support, optional onboard HDD, NO amc site, no Flash (ROHS 6/6)
ATCA-7368-L-CE	Commercial-ATCA blade, Intel Xeon E5620 4-CORE (2.4 GHZ), 0GB, 10G support, AMC SITE, no Flash (ROHS 6/6)
ATCA-7368-LSL-CE	Commercial-ATCA blade, Intel Xeon E5620 4-CORE (2.4 GHZ), 0GB, 10G support, optional onboard HDD, no AMC site, no Flash (ROHS 6/6)

As of printing date of this manual, the following board accessories are available.

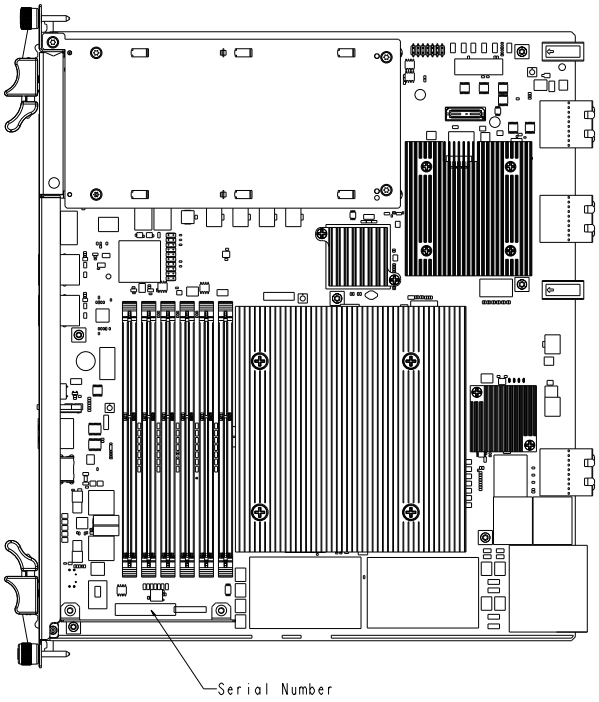
Table 1-4 Blade Accessories - Ordering Information

Accessory	Description
RTM-ATCA-7368	RTM for the ATCA-7368 with 1X slot for optional HDD (ROHS 6/6)

1.6 Product Identification

The following graphics shows the location of the serial number label.

Figure 1-5 Serial Number Location



Hardware Preparation and Installation

2.1 Overview

This chapter describes how to unpack and inspect the blade, environmental requirements, and how to install and remove the blade.

2.2 Unpacking and Inspecting the Blade

NOTICE

Damage of Circuits
Electrostatic discharge and incorrect blade installation and removal can damage circuits or shorten their life.
Before touching the blade or electronic components, make sure that you are working in an ESD-safe environment.

Shipment Inspection

To inspect the shipment, perform the following steps.

1. Verify that you have received all items of your shipment:
   - Printed *Quick Start Guide* and *Safety Notes Summary*
   - ATCA-7368 blade
   - Any optional items ordered

2. Check for damage and report any damage or differences to the customer service.
3. Remove the desiccant bag shipped together with the blade and dispose of it according to your country's legislation.

The blade is thoroughly inspected before shipment. If any damage occurred during transportation or any items are missing, please contact our customer's service immediately.

2.3 Environmental and Power Requirements

In order to meet the environmental requirements, the blade has to be tested in the system in which it is to be installed.

Before you power up the blade, calculate the power needed according to your combination of blade upgrades and accessories.

2.3.1 Environmental Requirements

The environmental conditions must be tested and proven in the shelf configuration used. The conditions refer to the surrounding of the blade within the user environment.

Table 2-1 Environmental Requirements

Requirement	Operating	Non-Operating
Temperature	Normal Operation: +5 °C (41 °F) to +40 °C (104 °F) according to Telcordia GR-63-CORE (NEBS) and ETSI EN 300 019-1-3, Class 3.1 Exceptional Operation: -5 °C (23 °F) to +55 °C (131 °F) according to Telcordia GR-63-CORE (NEBS) Note: This exceeds ETSI EN 300 019-1-3, Class 3.1E requirements (-5°C to +45°C)	-40 °C (-40 °F) to +70 °C (158 °F) according to Telcordia GR-63-CORE (NEBS) and ETSI EN 300 019-1-2, Class 2.3 Note: This exceeds ETSI EN 300 019-1-1, Class 1.2 requirements (storage from -25 °C to +55 °C Note: This may be further limited by installed accessories.
Temp. Change	+/- 0.25 °C/min according to Telcordia GR-63-CORE	+/- 0.25 °C/min
Rel. Humidity	Normal Operation: 5%rH to 85%rh non-condensing Exceptional Operation: 5%rH to 90%rh non-condensing According to Telcordia GR-63-CORE (NEBS) and EN 300 019-1-3, Classes 3.1 and 3.1E	5% to 95% non-condensing according to Telcordia GR-63-CORE (NEBS) and EN 300 019-1-1, Classes 1.2 and 2.3
Vibration	1g from 5 to 200Hz and back to 5Hz at a rate of 0.25 octave/minute (according to Telcordia GR-63-core)	5-20 Hz at 0.01 g^2/Hz (according to Telcordia GR-63-core and ETSI EN 300 019-2-2) 20-200 Hz at -3 dB/octave Hz (according to Telcordia GR-63-core and ETSI EN 300 019-2-2) Random 5-20Hz at 1 m^2/s^3 Random 20-200Hz at 3 m^2/s^3
Shock	Half-sine, 11 ms, 30 m/s^2	Blade level packaging Half-sine, 6 ms at 180 m/s^2

Table 2-1 Environmental Requirements (continued)

Requirement	Operating	Non-Operating
Free Fall	-	1.2 m/ packaged (according to ETSI 300 019-2-2) 100 mm unpackaged (according to Telcordia GR-63-core)

- The environmental requirements of the blade may be further limited down due to installed accessories, such as hard disks or AMC modules, with more restrictive environmental requirements.
- Operating temperatures refer to the temperature of the air circulating around the blade and not to the actual component temperature.

NOTICE

Blade Damage
Blade Surface
High humidity and condensation on the blade surface causes short circuits.
Do not operate the blade outside the specified environmental limits. Make sure the blade is completely dry and there is no moisture on any surface before applying power.

Blade Overheating and Blade Damage
Operating the blade without forced air cooling may lead to blade overheating and thus blade damage.
When operating the blade, make sure that forced air cooling is available on the shelf.

2.3.2 Power Requirements

The blade's power requirements depend on the installed hardware accessories. If you want to install accessories on the blade, the load of the respective accessory has to be added to that of the blade. In Table 2-2, you will find typical power requirements with and without accessories installed. For information on the accessories' power requirements, refer to the documentation delivered together with the respective accessory or consult your local Artesyn representative for further details.

The blade must be connected to a TNV-2 or a safety-extra-low-voltage (SELV) circuit. A TNV-2 circuit is a circuit whose normal operating voltages exceed the limits for a SELV circuit under normal operating conditions, and which is not subject to over voltages from telecommunication networks.

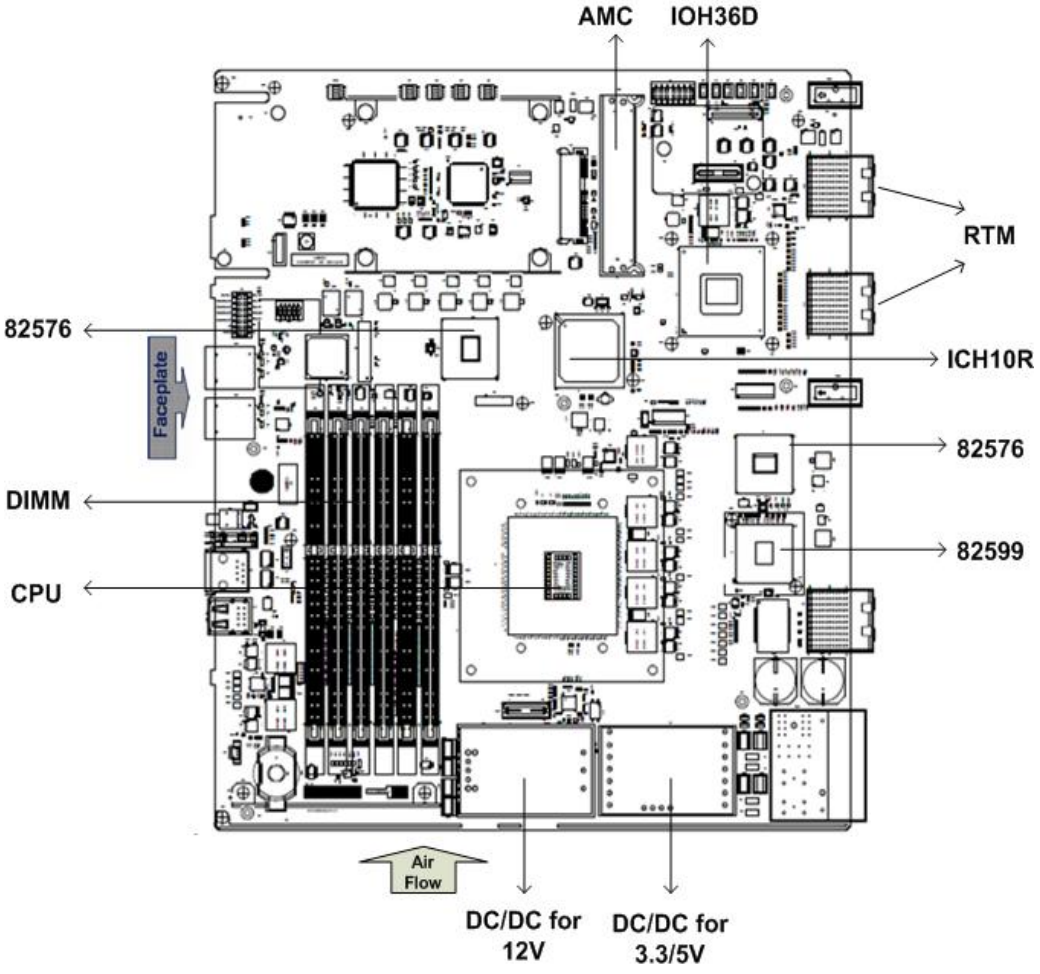
Table 2-2 Power Requirements

Characteristic	Value
Max. power consumption of ATCA-7368	145 W

2.4 Blade layout

Figure 2-1 illustrates the ATCA-7368 blade layout.

Figure 2-1 Blade Layout



2.5 Installing the Blade Accessories

The following additional components are available for the blade:

- DIMM memory modules
- PMEM (persistent memory) module
- SATA module
- USB flash module
- Rear transition modules
- AMC module

They are described in detail in the following sections. For order numbers refer to section *Ordering Information* on page 39.

2.5.1 DIMM Memory Modules

The blade provides six memory slots for main memory DIMM modules. You may install and/or remove DIMM memory modules in order to adapt the main memory size to your needs. The corresponding installation/removal procedures are described in this section.

The location of the DIMM Memory Modules are shown in Figure "Blade Layout" on page 46.

When installing DIMM memory modules, the DIMM sockets farthest away on each memory channel from the CPU device need to be populated first. Only qualified DDR3 DIMMs (Dual Ranked RDIMM) are allowed.

ATCA-7368 supports low-voltage DDR3 memory. This is available upon request.

DIMM modules used within one channel must be based on the same memory technology. For maximum memory performance all three channels of one CPU must be equipped with an identical amount and size of DIMMs.

NOTICE

Damage of Circuits
Electrostatic discharge and incorrect module installation and removal can damage circuits or shorten their life.
Before touching the module or electronic components, make sure that you are working in an ESD-safe environment.

Installation Procedure

To install a DIMM module, proceed as follows:

1. Remove blade from system as described in *Installing and Removing the Blade* on page 52.
2. Open locks of memory module socket.
3. Press module carefully into socket.
   As soon as the memory module has been fully inserted, the locks automatically close.
4. If applicable, repeat steps 2 to 3 to install further modules.

NOTICE

Damage of Circuits
Electrostatic discharge and incorrect module installation and removal can damage circuits or shorten their life.
Before touching the module or electronic components, make sure that you are working in an ESD-safe environment.

Removal Procedure

To remove a DIMM module, proceed as follows:

1. Remove blade from system as described in *Installing and Removing the Blade* on page 52.
2. Open locks of socket at both sides.
   The memory module is automatically lifted up.
3. Remove module from socket.
4. Repeat steps 2 to 3 in order to remove further memory modules.

2.5.2 PMEM and SATA Module

The PMEM/SATA extension slot allows assembly of either a PMEM or SATA module which are available as upgrade kits for ATCA-7368. The PMEM module consists of an SRAM and a flash memory. The SRAM has a capacity of up to 16 MB and can be used as persistent memory, i.e. a memory that holds up the contents during reset. The flash memory has a capacity of up to 64 MB organized as two memory banks. The S/F memory module connects to the blade's PCI subsystem. It can be configured via an FPGA register.

The SATA module consists of a Solid State Disc of up to 128 GB and a SATA controller and connects physically to ICH10 SATA Port #5.

The extension module is mechanically fastened to the blade with two screws. The location of the two corresponding mounting holes as well as the S/F memory module connector is shown in Figure "Blade Layout" on page 46.

The PMEM and SATA module are accessory kits and are not part of the default ATCA-7368. The following procedure describes the steps to install/remove the PMEM/SATA module.

Installation Procedure

To install a PMEM/SATA module, proceed as follows:

NOTICE

Damage of Circuits
Electrostatic discharge and incorrect module installation and removal can damage circuits or shorten their life.
Before touching the module or electronic components, make sure that you are working in an ESD-safe environment.

1. Remove the blade from the system as described in *Installing and Removing the Blade* on page 52.
2. Plug the PMEM/SATA module on the blade so that the module's standoffs fit in the blade's mounting holes.
3. Fasten the PMEM/SATA module to the blade using the two screws that previously had fixed the S/F memory module to the blade.
4. Reinstall the blade into the system as described in *Installing and Removing the Blade* on page 52.
   The additional resource (either memory or SATA SSD) will be detected automatically during the boot-up sequence.

Removal Procedure

To remove a PMEM/SATA module, proceed as follows:

NOTICE

Damage of Circuits
Electrostatic discharge and incorrect module installation and removal can damage circuits or shorten their life.
Before touching the module or electronic components, make sure that you are working in an ESD-safe environment.

1. Remove the blade from the system as described in *Installing and Removing the Blade* on page 52.
2. Remove the two screws holding the PMEM/SATA module.
3. Remove the PMEM/SATA module from the blade.
4. Reinstall the blade into the system as described in *Installing and Removing the Blade* on page 52.

2.5.3 USB 2.0 Flash Module

The blades provides a USB 2.0 flash module with a capacity of 4 GB or 16 GB. The corresponding removal/installation procedures are described in this section.

The location of the USB 2.0 Flash Module is shown in Figure "Blade Layout" on page 46.

NOTICE

Damage of Circuits
Electrostatic discharge and incorrect module installation and removal can damage circuits or shorten their life.
Before touching the module or electronic components, make sure that you are working in an ESD-safe environment.

Removal Procedure

To remove a USB flash module, proceed as follows:

1. Remove blade from system as described in *Removing the Blade* on page 56.
2. Remove the screw on the left side of the flash module.
3. Lift the flash module from the socket.

Installation Procedure

To install a USB flash module, proceed as follows:

1. Remove blade from system as described in *Removing the Blade* on page 56.
2. Insert new flash module in socket.
3. Tighten the screw on the left side of the flash module.

2.6 Installing and Removing the Blade

The blade is fully compatible to the AdvancedTCA standard and is designed to be used in AdvancedTCA shelves.

The blade can be installed in any AdvancedTCA node slot. Do not install it in an AdvancedTCA hub slot.

NOTICE

Damage of Circuits
Electrostatic discharge and incorrect blade installation and removal can damage circuits or shorten their life.
Before touching the blade or electronic components, make sure that you are working in an ESD-safe environment.

Blade Malfunctioning
Incorrect blade installation and removal can result in blade malfunctioning.
When plugging the blade in or removing it, do not press on the faceplate but use the handles.

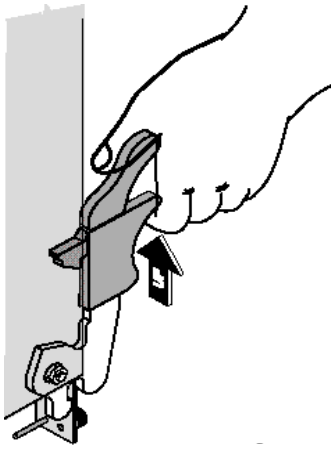
2.6.1 Installing the Blade

To install the blade into an AdvancedTCA shelf, proceed as follows.

Installation Procedure

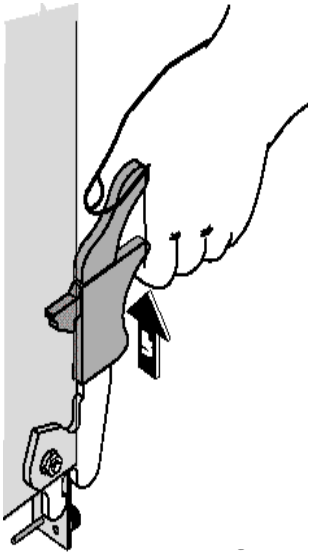
The following procedure describes the installation of the blade. It assumes that your system is powered on. If your system is not powered on, you can disregard the blue LED and thus skip the respective step. In this case, it is purely a mechanical installation.

1. Ensure that the top and bottom ejector handles are in the outward position by squeezing the lever and the latch together.



2. Insert blade into the shelf by placing the top and bottom edges of the blade in the card guides of the shelf. Ensure that the guiding module of shelf and blade are aligned properly.
3. Apply equal and steady pressure to the blade to carefully slide the blade into the shelf until you feel resistance. Continue to gently push the blade until the blade connectors engage.
4. Squeeze the lever and the latch together and hook the lower and the upper handle into the shelf rail recesses.

5. Fully insert the blade and lock it to the shelf by squeezing the lever and the latch together and turning the handles towards the faceplate.



If your shelf is powered on, as soon as the blade is connected to the backplane power pins, the blue LED is illuminated.
When the blade is completely installed, the blue LED starts to blink. This indicates that the blade announces its presence to the shelf management controller.

If an RTM is connected to the front blade, make sure that the handles of both the RTM and the front blade are closed in order to power up the blade's payload.

6. Wait until the blue LED is switched off, then tighten the faceplate screws which secure the blade to the shelf.
   The switched off blue LED indicates that the blade's payload has been powered up and that the blade is active.

7. Connect cables to the faceplate, if applicable.

2.6.2 Removing the Blade

This section describes how to remove the blade from an AdvancedTCA system.

NOTICE

Damage of Circuits
Electrostatic discharge and incorrect blade installation and removal can damage circuits or shorten their life.
Before touching the blade or electronic components, make sure that you are working in an ESD-safe environment.

Blade Malfunctioning
Incorrect blade installation and removal can result in blade malfunctioning.
When plugging the blade in or removing it, do not press on the faceplate but use the handles.

Removal Procedure

The following procedure describes how to remove the blade from a system. It assumes that the system is powered on. If the system is not powered on, you can disregards the blue LED and thus skip the respective step. In that case, it is purely a mechanical procedure.

1. Unlatch the lower handle by squeezing the lever and the latch together and turning the handle outward just enough to unlatch the handle from the faceplate. Do not rotate the handle fully outward.
   The blue LED blinks indicating that the blade power-down process is ongoing.
2. Wait until the blue LED is illuminated permanently, then unlatch the upper handle and rotate both handles fully outward.

If the LED continues to blink, a possible reason may be that the upper layer software rejected the blade extraction request.

NOTICE

Data Loss
Removing the blade with the blue LED still blinking causes data loss.
Wait until the blue LED is permanently illuminated, before removing the blade.

3. Remove the faceplate cables, if applicable.
4. Unfasten the screws of the faceplate until the blade is detached from the shelf.
5. Remove the blade from the shelf.

3.1 Overview

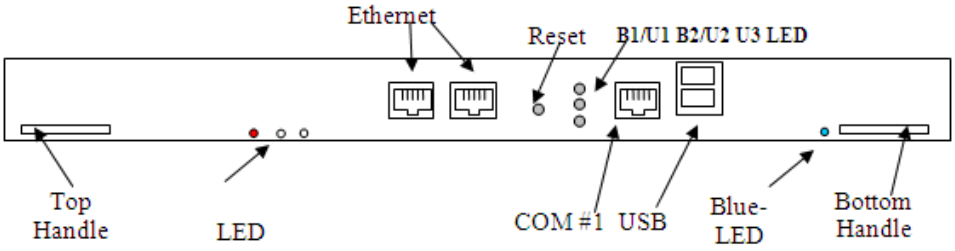
This chapter describes the LEDs, connectors, and external interfaces of the board.

3.2 Faceplate

The following figure shows the connectors, keys, and LEDs available at the Faceplate.

The blade design provides the possibility to cover unused Faceplate elements like LEDs or push buttons behind a custom overlay foil. The following figure gives an overview of the ATCA-7368 faceplate features.

Figure 3-1 Faceplate



3.2.1 LEDs and Interfaces

The blade's faceplate provides the following interfaces and control elements:

- Two USB 2.0 ports
- Serial console port to connect to either payload or IPMC serial I/F
- Out of Service, In Service, Attention, and Hot Swap LEDs (IPMC control)

- Two Ethernet ports
- Recessed reset button

Figure 3-2 Faceplate LEDs

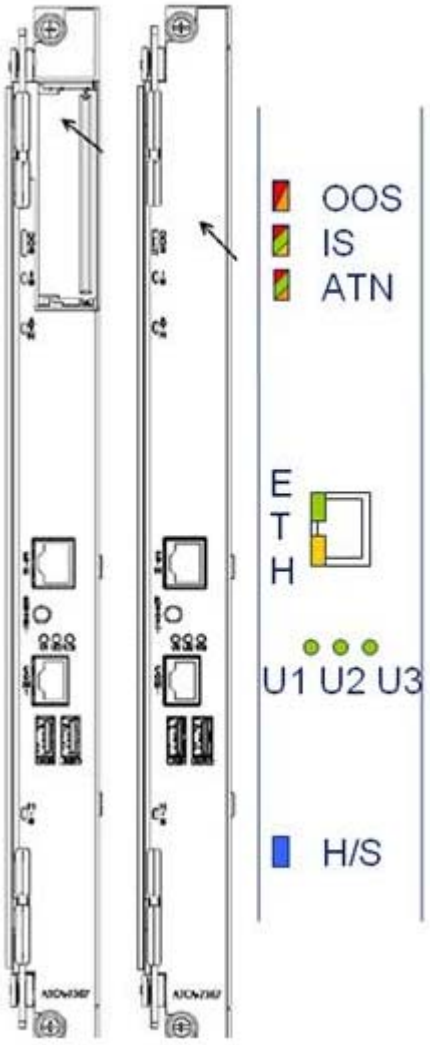


Table 3-1 provides the description of the LEDs.

Table 3-1 Faceplate LEDs

Indicator	Color	Description
Out of Service ATCA LED1	Red or Amber	Out of Service Red/ optional Amber (controlled by IPMC): This LED is controlled by higher layer software such as middleware or applications. Red: On after power up and lamp test finished
In Service ATCA LED2	Red, Green or Yellow	In Service Red/green/yellow (controlled by IPMC): This LED is controlled by higher layer software such as middleware or applications. Off after power up and lamp test finished
Attention ATCA LED3	Amber	Attention Amber: This LED is controlled by higher layer software such as middleware or applications. Off after power up and lamp test finished
Ethernet Status LEDs	Green, Yellow	The Ethernet connector provides two status LEDs: ● Link (upper) – Green: Link is available – Off: No link ● Activity (lower) – Yellow: Activity – Off: No activity
U1, U2, U3	Red, Green, Amber	U1, U2: ● Red: during BIOS boot ● Green: Base interface activity U3 ● User defined LED

Table 3-1 Faceplate LEDs (continued)

Indicator	Color	Description
Hot Swap	Blue	FRU State Machine ● During blade installation – Blue: Onboard IPMC powers up – Blue (blinking): Blade is communicating with the shelf manager – Off: Blade is active ● During blade removal – Blue (blinking): Blade is notifying the shelf manager that it is going to deactivate – Blue: Blade is ready to be extracted

Base-IF and faceplate Ethernet activity can be seen through FPGA LEDs B1/U1, B2/U2 and U3.

3.2.2 Connectors

3.2.2.1 Faceplate Connectors

Table 3-2 RJ45 female Serial Line Connector Pinout

Pin	Signal
1	RTS
2	DTR
3	TXD
4	GND
5	GND
6	RXD
7	DSR
8	CTS

Table 3-3 USB Connector Pinout

Pin	Signal
1	VP5_USB
2	USB_x_D-
3	USB_x_D+
4	GND

Table 3-4 10/100/1000Base-T Fast Ethernet Connector Pinout

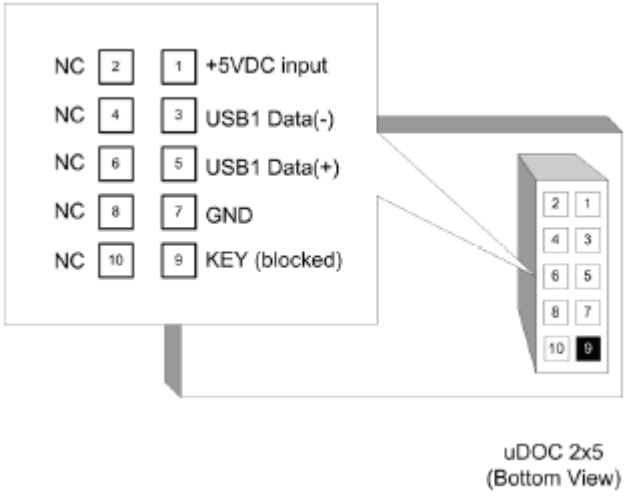
Pin	Signal
1	ETH_TX+
2	ETH_TX-
3	ETH_RX+
4	
5	
6	ETH_RX-
7	
8	

3.3 Onboard Connectors

3.3.1 USB2.0 FLASH Connector

One USB Port of ICH10R is connected to the onboard USB Flash Disk Module.

Figure 3-3 USB2.0 Flash Disk module connector pinout



3.3.2 Backplane Connectors

Table 3-5 Zone 1 Connector P1 Pin Assignment

Contact Number	Destination	Description
1 - 4	Reserved	Reserved
5	IPMC ISC PC0	Hardware Address Bit 0
6	IPMC ISC PC1	Hardware Address Bit 1
7	IPMC ISC PC2	Hardware Address Bit 2

Table 3-5 Zone 1 Connector P1 Pin Assignment

Contact Number	Destination	Description
8	IPMC ISC PC3	Hardware Address Bit 3
9	IPMC ISC PD4	Hardware Address Bit 4
10	IPMC ISC PD5	Hardware Address Bit 5
11	IPMC ISC PD6	Hardware Address Bit 6
12	IPMC ISC PD7	Hardware Address Bit 7
13	IPMC IMC PD0	IPMB Clock Port A
14	IPMC IMC PD1	IPMB Data Port A
15	IPMC ISC PC5	IPMB Clock Port B
16	IPMC ISC PC4	IPMB Data Port A
17 - 24	Not used	Not used
25	Shelf Ground	Shelf Ground
26	Logic Ground	Logic Ground
27	Power Building Block	Enable B
28	Power Building Block	Voltage Return A
29	Power Building Block	Voltage Return B
30	Power Building Block	Early -48V A
31	Power Building Block	Early -48V B
32	Power Building Block	Enable A
33	Power Building Block	-48V A
34	Power Building Block	-48V A

Table 3-6 Zone 2 Connector P23 Pin Assignment

P23									
Row #	Interface	Col AB		Col CD		Col EF		Col GH	
1	Fabric Channel 2	F2[2]_ TX+	F2[2]_ TX-	F2[2]_ RX+	F2[2]_ RX-	F2[3]_ TX+	F2[3]_ TX-	F2[3]_ RX+	F2[3]_ RX-
2		F2[0]_ TX+	F2[0]_ TX-	F2[0]_ RX+	F2[0]_ RX-	F2[1]_ TX+	F2[1]_ TX-	F2[1]_ RX+	F2[1]_ RX-

Table 3-6 Zone 2 Connector P23 Pin Assignment (continued)

P23									
3	Fabric Channel 1	F1[2]_ TX+	F1[2]_ TX-	F1[2]_ RX+	F1[2]_ RX-	F1[3]_ TX+	F1[3]_ TX-	F1[3]_ RX+	F1[3]_ RX-
4		F1[0]_ TX+	F1[0]_ TX-	F1[0]_ RX+	F1[0]_ RX-	F1[1]_ TX+	F1[1]_ TX-	F1[1]_ RX+	F1[1]_ RX-
5	Base Channel 1	BI1_D A+	BI1_D A-	BI1_DB +	BI1_D B-	BI1_D C+	BI1_D C-	BI1_D D+	BI1_D D-
6	Base Channel 2	BI2_D A+	BI2_D A-	BI2_DB +	BI2_D B-	BI2_D C+	BI2_D C-	BI2_D D+	BI2_D D-
7	n/a	NC	NC	NC	NC	NC	NC	NC	NC
8	n/a	NC	NC	NC	NC	NC	NC	NC	NC
9	n/a	NC	NC	NC	NC	NC	NC	NC	NC
10	n/a	NC	NC	NC	NC	NC	NC	NC	NC

3.3.3 Zone 3

The ATCA specification defines Zone 3 for user input/output signals. On ATCA-7368, ATCA Zone 3 Type A connector (direct connect to RTM) is used. The same connectors are used for Zone 2 and Zone 3. Zone 3 connectors are assigned to reference designators P30 through P32.

Zone 3 Connector P30 is the top most connector, P31 is below P30 and P32 is below P31. Zone 3 connectors carry the following I/O interface signals:

- 1x Serial Line COM#0 from Glue Logic FPGA
- RST Button RTM Faceplate
- USB
- Serial ATA
- 4 x PCIexpress X4 and one x2 lane width each with individual clock
- IPMB-L
- Debugging
- Management Power +3.3V
- Payload Power +12V

4.1 Overview

The Basic Input Output System (BIOS) provides an interface between the operating system and the hardware of the blade. It is used for hardware configuration. Before loading the operating system, BIOS performs basic hardware tests and prepares the blade for the initial boot-up procedure.

During blade production, identical BIOS images are programmed into both boot flash banks. It is possible to select boot flash as device to boot from. This is done via an IPMI command. For further details refer to section *Supported IPMI Commands* on page 103.

The BIOS used on the blade is based on the AMI UEFI BIOS with several Artesyn extensions integrated. Its main features are:

- Initialize CPU, chipset and memory
- Initialize PCI devices
- Setup utility for setting configuration data
- IPMC support
- Serial console redirection for remote blade access
- Boot operation system

The BIOS complies with the following specifications:

- UEFI Specification 2.0
- Plug and Play BIOS Specification 1.0A
- PCI BIOS Specification 2.1
- SMBIOS Specification 2.3
- BIOS Boot Specification 1.01
- PXE 2.1

- SMP 1.4
- ACPI 3.0b

The BIOS contains online documentation which describes in detail the available menu options. Therefore, the description in this manual is limited to the main BIOS functions.

The BIOS setup program is required to configure the blade hardware. This configuration is necessary for operating the blade and connected peripherals. The configuration data are stored in the same flash device from which the board boots.

When you are not sure about configuration settings, restore the default values. This option is provided in case a value has been changed and you wish to reset settings. To restore the default values, press <F3> in Setup.

- Loading the BIOS default values will affect all set-up items and will reset options previously altered.
- If you set the default values, the displayed default values takes effect only after the BIOS setup is saved and closed.

4.2 Accessing the Blade using the Serial Console Redirection

The blade firmware provides a serial console redirection feature allowing remote access to the blade through a terminal connected to the blade's serial interface.

The terminal can be connected to display VGA text information. Terminal keyboard input is redirected and treated as a normal PC keyboard input. The serial console redirection feature can be configured via a setup utility.

4.2.1 Requirements

For serial console redirection, the following is required:

- Terminal or terminal emulation which supports a VT100 or ANSI mode
- NULL-modem cable

Terminal emulation programs such as TeraTermPro can be used. In order to use TeraTermPro using the function keys, the keyboard configuration file of TeraTermPro has to be modified as follows:

Table 4-1 BIOS Key Codes for Terminal Emulation Program

Function Key	Key Code
PF1	59
PF2	60

4.2.2 Default Access Parameters

By default, the blade can be accessed using the serial interface COM1. This interface is using a RJ-45 connector at the blade's Faceplate.

A NULL-Modem cable is available as accessory kit for the blade. It converts the RJ-45 connector to a standard DSUB connector which can be connected to a remote terminal. The following communication parameters are used, by default:

- Baud rate: 38400
- Flow control: None
- VT-100
- 8 data bits
- No parity
- 1 stop bit

4.2.3 Connecting to the Blade

Procedure

In order to connect to the blade using the serial console redirect feature, proceed as follows:

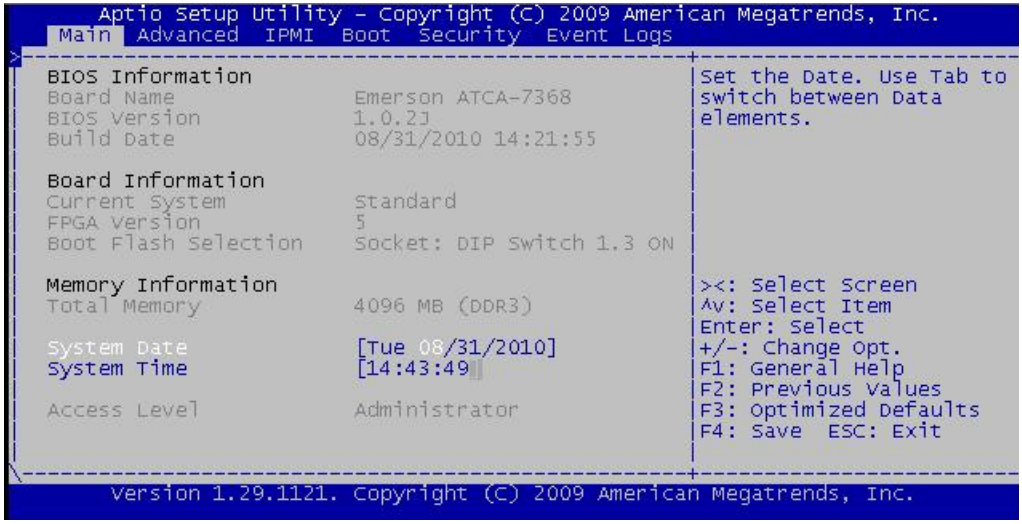
1. Configure terminal to communicate using the same parameters as in BIOS setup.
2. Connect terminal to NULL-modem cable.
3. Connect NULL-modem cable to COM port of the blade.
4. Start up blade.

4.3 Changing Configuration Settings

When the system is turned on or rebooted, the presence and functionality of the system components is tested by POST (Power-On Self-Test).

Press <F2> when requested. The main menu appears. It looks similar to the one shown in the following figure.

Figure 4-1 Main Menu



- Make sure that BIOS is properly configured prior to installing the operating system and its drivers.
- If you save changes in setup, the next time the blade boots BIOS will configure the system according to the setup selections stored. If those values cause the system boot to fail, reboot and enter setup to get the default values or to change the selections that caused the failure.

In order to navigate in setup, use the arrow keys on the keyboard to highlight items on the menu. All other navigation possibilities are shown at the bottom of the menu.

Additionally, an item-specific help is displayed on the right side of the menu window.

4.4 Boot Options

This section describes which boot devices are supported by the BIOS and how to select the boot device.

4.4.1 Supported Boot Devices

The BIOS supports booting from the following devices/sources:

- USB Devices (Sticks, onboard embedded USB flash disk, Hard Drives, CD-ROM)
- SAS controller on ARTM
- Fibre Channel Controller on ARTM
- Network (BEV)
- AMC SATA & SAS HDD
- Onboard embedded SDD

Default boot order:

- Attached USB CDROM
- Removable dev (if applicable)
- Attached USB devices of USB external port
- SAS HDD connected to ARTM SAS Controller
- Base Ethernet Interface
- EFI shell

In case BIOS does not find any ready bootable device, it may loop on the source list until any boot device becomes ready or watchdog bites.

4.4.2 Selecting The Boot Device

There are two possibilities to determine the device from which BIOS attempts to boot:

- By setup to select a permanent order of boot devices
- By boot selection menu to select any device for the next boot-up procedure only

By Setup

To select the boot device by setup, proceed as follows:

1. From the menu, select [Boot].
2. Select the order of the devices from which BIOS attempts to boot the operating system.
3. Enter the submenu "Option Rom Execution" to enable/disable booting from specific devices. Changes have to be saved and the board has to be rebooted when changing the Option Rom Execution.

If BIOS is not successful at booting from one device, it tries to boot from the next device on the list.

4.4.3 By Boot Selection Menu

1. From the menu, select [Save & Exit].
2. Override existing boot sequence by selecting another boot device from the boot override list.

If the selected device does not load the operating system, BIOS resets the board and reverts to the previous boot sequence.

4.4.4 Network boot

Initially the BIOS will contain a classic PXE OPROMs. In later project phase if required the BIOS will contain also the UEFI Network Device Driver which allows the loading of executable code from a network server. Both, DHCP and BOOTP protocols are supported for obtaining an IP address. File transmission is accomplished via the TFTP protocol. The UEFI Network Device Driver is intellectual property of INTEL Corp. If possible a BIOS setup item will be available to enable/disable the UEFI Network Device Driver. In Boot menu displayed Network boot device names will be changed to be User friendly if required.

The following table summarizes the network boot support status:

Table 4-2 Network Boot Support Status

Ethernet Interface	PXE Boot Support
Front Panel Network Interface 1 (82576EB - 1)	YES
Front Panel Network Interface 2 (82576EB - 2)	YES
Base Network Interface 1 (82576EB - 1)	YES
Base Network Interface 2 (82576EB - 2)	YES
Fabric Network Interface 1 (82599EB - 1)	YES
Fabric Network Interface 2 (82599EB - 2)	YES
1 x 82576EB, total 2 GbE interfaces on RTM	YES

4.5 Redirection of I/O

4.5.1 Redirection of the I/O to COM ports (Console Redirection)

Redirection of I/O to a COM port makes it possible to control the ATCA-7368 BIOS in an embedded environment where no VGA adapter is present and no keyboard is attached. The following options are configurable via BIOS setup:

- Baudrate
  9600 baud, 19200 baud, 38400 baud, and 115200 baud are supported. The default value is 38400 baud.
- COM1port
  Gives the user the possibility to select either of the onboard serial port or to disable the console redirection.
  Possible settings: enabled, disabled.
  The default value is enabled. If disabled is selected, no redirection of I/O to a COM port will be performed. COM1 is fully compliant to industry standard 16550 asynchronous communication controllers and is integrated in the Glue Logic FPGA.

4.6 LED behavior during POST

After power up/reset and while BIOS runs the LEDs are used to signalize the power up/ BIOS phases. The state of LEDs is defined so that in case of a hang the LEDs clearly indicate in which boot up phase the hang occurred. In general, to indicate that the POST is in progress, the BIOS toggles the user LED for every POST task it executes. After the POST has been completed, the BIOS switches off the LEDs. The LEDs marked with B1/U1,B2/U2 and U3 will be used for this purpose.

From the OS/BBS_application_sw layer, when the blade successfully boots up in to PNE Linux, the BBS application will:

1. Switch the OOS LED off
2. Switch the IS LED on
3. Switch the ATN LED off

When the blade is shutting down gracefully from PNE Linux OS, the BBS application will:

1. Switch the OOS LED on
2. Switch the IS LED off
3. Switch the ATNLED off

4.7 LED Usage

The BIOS uses LEDs U1, U2 and U3 on the front panel to indicate activity of startup progress. In boot loader phase (PEI phase), U1 and U2 glow red, U3 is glowing alternately red, green and orange.

In the main initialization phase (DXE phase), only U3 is glowing alternately red, green and orange. U1 and U2 are set to the default value: base Ethernet interface link and activity LEDs. Short before leaving BIOS and staring an operating system, LED U3 is set to green.

4.8 RTM SAS Controller

The BIOS extension firmware supports RAID 0 and RAID 1.

4.9 Board Information Display

The BIOS shall display the following Board related information in BIOS Setup under “Board Info”:

- Current System (label for the loaded BIOS defaults set)
- BIOS Version
- BIOS Date
- IPMI Firmware Version
- FPGA Version (Onboard FPGA version)
- BIOS Source (boot flash device bank)
- CPU information
- CPLD information
- Board Serial Number stored in IPMI FRU data

4.10 USB Ports

The USB ports can be disabled by BIOS setup menu.

Table 4-3 USB Ports

USB port BIOS setting	Format/Options	Default Value
Onboard USB FlashDisk	Enabled/Disabled	Enabled
Front Panel USB	Enabled/Disabled	Enabled
ARTM USB	Enabled/Disabled	Enabled

4.11 Supported Operating Systems

WRS PNE LE 4.x Linux, Red Hat Enterprise Linux 5.x will be supported. DOS will be used for debugging.

4.12 Persistent Memory Module

The Artesyn SFMEM-MODULE (P/N #122265) persistent memory module can be attached to ATCA-7368. If attached the BIOS will automatically initialize the PCI bridge on the SFMEM-MODULE during normal PCI initialization BIOS phase. There will be no BIOS Setup items related to SFMEM-MODULE.

4.13 Upgrading the BIOS

A BIOS upgrade kit for the blade is available. This allows the BIOS to be upgraded. The BIOS upgrade kit contains documentation which describes in detail how to upgrade the BIOS.

Update tool for Linux is provided with Basic Blade Services (BBS). For details on how to upgrade BIOS from Linux, refer *Basic Blade Services Software for the ATCA-7368 Programmer's Reference*.

After performing a BIOS upgrade or after restoring a corrupted BIOS image, all BIOS settings are reset to their default values except for parameters that are stored in IPMC storage area.

4.14 BIOS Error Messages

In some cases, the BIOS prints error messages to the console. For example, an error message is printed when the CMOS battery is bad or was removed. In case of memory errors, BIOS disables the defective DIMM module and prints a message similar to the one below and continues:

```
Memory Error Detected: Disable DIMM 0 Channel 1 Node 0 (DIMM Socket
P03)
ERROR: Minor (40) ComputingUnit (0) Memory (5): None Useful (100a)
```

In this example, the DIMM module in socket P03 is disabled.

When BIOS does not find useful memory, it prints the following message and stops.

```
FATAL ERROR: No Memory Found (E8/01)
ERROR: Major (80) ComputingUnit (0) Memory (5): None Detected (1009)
```

4.15 BIOS Status Codes

The following table lists the BIOS status codes applicable to the used AMI UEFI BIOS. The BIOS status codes are stored in the blade's Port 80 register and can also be obtained by reading an on-board IPMI sensor.

4.15.1 Status Code Ranges

Table 4-4 Status Code Ranges

Status Code Range	Description
0x01 – 0x0F	SEC Status Codes & Errors
0x10 – 0x2F	PEI execution up to and including memory detection
0x30 – 0x4F	PEI execution after memory detection
0x50 – 0x5F	PEI errors
0x60 – 0xCF	DXE execution up to BDS
0xD0 – 0xDF	DXE errors
0xE0 – 0xE8	S3 Resume (PEI)
0xE9 – 0xEF	S3 Resume errors (PEI)
0xE8 - 0xEF	Memory initialization errors
0xB0 - 0xBF	Additional Memory Initialization Status Codes
0xE8 - 0xEE	Additional Memory Error Status Codes

4.15.2 Standard Status Codes

Table 4-5 SEC Status Codes

Status Code	Description
0x0	Not used

Table 4-5 SEC Status Codes (continued)

Status Code	Description
Progress Codes	
0x1	Power on. Reset type detection (soft/hard).
0x2	AP initialization before microcode loading
0x3	North Bridge initialization before microcode loading
0x4	South Bridge initialization before microcode loading
0x5	OEM initialization before microcode loading
0x6	Microcode loading
0x7	AP initialization after microcode loading
0x8	North Bridge initialization after microcode loading
0x9	South Bridge initialization after microcode loading
0xA	OEM initialization after microcode loading
0xB	Cache initialization
SEC Error Codes	
0xC – 0xD	Reserved for future AMI SEC error codes
0xE	Microcode not found
0xF	Microcode not loaded

Table 4-6 PEI Status Codes

Status Code	Description
Progress Codes	
0x10	PEI Core is started
0x15	Pre-memory North Bridge initialization is started
0x19	Pre-memory South Bridge initialization is started
0x2F	Memory initialization (other)
0x31	Memory Installed
0x32	CPU post-memory initialization is started
0x33	CPU post-memory initialization. Cache initialization

Table 4-6 PEI Status Codes (continued)

Status Code	Description
0x34	CPU post-memory initialization. Application Processor(s) (AP) initialization
0x35	CPU post-memory initialization. Boot Strap Processor (BSP) selection
0x36	CPU post-memory initialization. System Management Mode (SMM) initialization)
0x37	Post-Memory North Bridge initialization is started
0x3B	Post-Memory South Bridge initialization is started
0x3F-0x4E	OEM post memory initialization codes
0x4F	DXE IPL is started
Memory Initialization Codes	
0xB0	Chipset initialization
0xB1	Detect reset state
0xB2	DIMM detect
0xB3	Clock initialization
0xB4	Read SPD data
0xB5	Early memory controller initialization
0xB6	Check DIMM population
0xB7	Channel initialization
0xB8	Channel training
0xB9	Run Build In Self Test
0xBA	Initialize memory map
0xBB	Setup RAS configuration
0xBF	Memory initialization complete
PEI Error Codes	
0x53	Memory initialization error. No usable memory detected
0x55	Memory not installed
0x56	Invalid CPU type or Speed

Table 4-6 PEI Status Codes (continued)

Status Code	Description
0x57	CPU mismatch
0x58	CPU self test failed or possible CPU cache error
0x59	CPU micro-code is not found or micro-code update is failed
0x5A	Internal CPU error
0x5B	Reset PPI is not available
Memory Error Codes	
0xE8	No Memory
0xEA	DDR initialization error
0xEB	Memory test error
0xED	Mixed memory types
0xEE	Population error
Recovery Progress Codes	
0xF0	Recovery condition triggered by firmware (Auto recovery)
0xF1	Recovery condition triggered by user (Forced recovery)
0xF2	Recovery process started
0xF3	Recovery firmware image is found
0xF4	Recovery firmware image is loaded
0xF5-0xF7	Reserved for future AMI progress codes
Recovery Error Codes	
0xF8	Recovery PPI is not available
0xF9	Recovery capsule is not found
0xFA	Invalid recovery capsule
0xFB – 0xFF	Reserved for future AMI error codes

Table 4-7 DXE Status Codes

Status Code	Description
0x60	DXE Core is started
0x61	NVRAM initialization
0x62	Installation of the South Bridge Runtime Services
0x63	CPU DXE initialization is started
0x68	PCI host bridge initialization
0x69	North Bridge DXE initialization is started
0x6A	North Bridge DXE SMM initialization is started
0x70	South Bridge DXE initialization is started
0x71	South Bridge DXE SMM initialization is started
0x72	South Bridge devices initialization
0x78	ACPI module initialization
0x79	CSM initialization
0x90	Boot Device Selection (BDS) phase is started
0x91	Driver connecting is started
0x92	PCI Bus initialization is started
0x93	PCI Bus Hot Plug Controller Initialization
0x94	PCI Bus Enumeration
0x95	PCI Bus Request Resources
0x96	PCI Bus Assign Resources
0x97	Console Output devices connect
0x98	Console input devices connect
0x99	Super IO Initialization
0x9A	USB initialization is started
0x9B	USB Reset
0x9C	USB Detect
0x9D	USB Enable
0xA0	IDE initialization is started

Table 4-7 DXE Status Codes (continued)

Status Code	Description
0xA1	IDE Reset
0xA2	IDE Detect
0xA3	IDE Enable
0xA4	SCSI initialization is started
0xA5	SCSI Reset
0xA6	SCSI Detect
0xA7	SCSI Enable
0xA8	Setup Verifying Password
0xA9	Start of Setup
0xAB	Setup Input Wait
0xAD	Ready To Boot event
0xAE	Legacy Boot event
0xAF	Exit Boot Services event
0xB0	Runtime Set Virtual Address MAP Begin
0xB1	Runtime Set Virtual Address MAP End
0xB2	Legacy Option ROM Initialization
0xB3	System Reset
0xB4	USB hot plug
0xB5	PCI bus hot plug
0xB6	Clean-up of NVRAM
0xB7	Configuration Reset (reset of NVRAM settings)
DXE Error Codes	
0xD0	CPU initialization error
0xD1	North Bridge initialization error
0xD2	South Bridge initialization error
0xD3	Some of the Architectural Protocols are not available
0xD4	PCI resource allocation error. Out of Resources

Table 4-7 DXE Status Codes (continued)

Status Code	Description
0xD5	No Space for Legacy Option ROM
0xD6	No Console Output Devices are found
0xD7	No Console Input Devices are found
0xD8	Invalid password
0xD9	Error loading Boot Option (LoadImage returned error)
0xDA	Boot Option is failed (StartImage returned error)
0xDB	Flash update is failed
0xDC	Reset protocol is not available

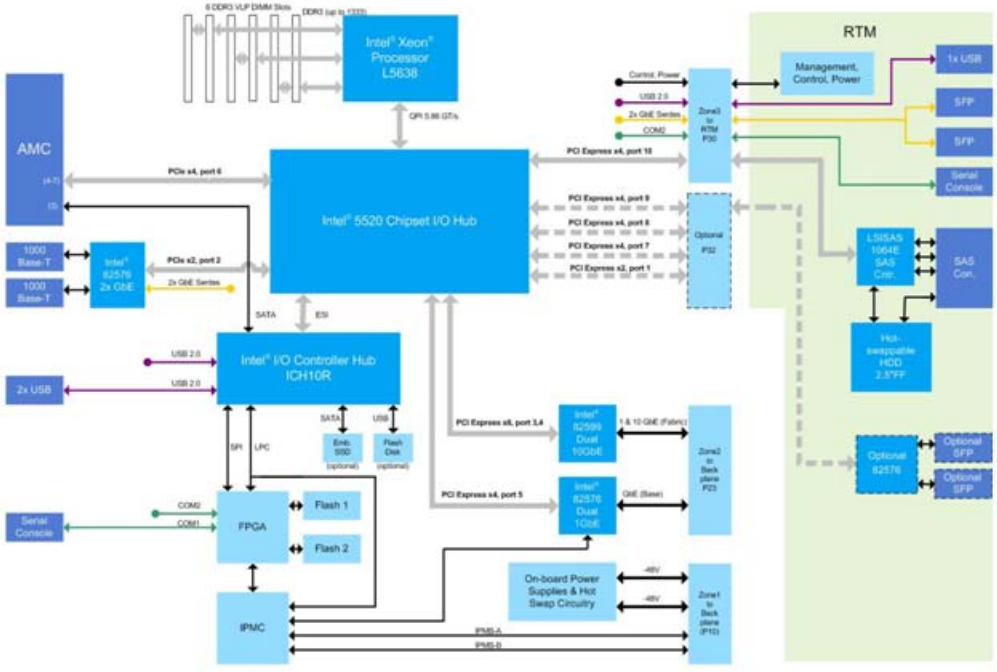
5.1 Overview

This chapter describes the specifications and functions of the ATCA-7368 blade.

5.2 Block Diagram

Figure 5-1 shows the block diagram of ATCA-7368 blade.

Figure 5-1 Block Diagram

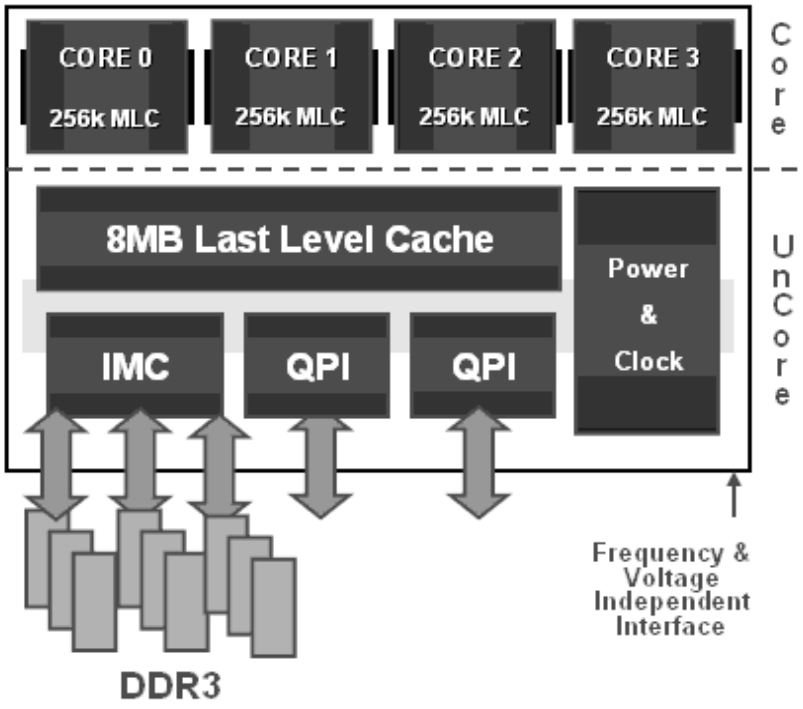


5.3 Processor

Westmere-EP processor is a Six-core processor, based on 32 nm process technology first implementation of the Intel Nehalem ™ Micro architecture. The processor family features a range of thermal design power (TDP) envelopes from 40W TDP up to 130W TDP. The processor features two Intel QuickPath Interconnect point-to-point links capable of up to 6.4GT/S, 12MB of shared Last Level cache (L3), and an Integrated Memory Controller (IMC). The processor support all the existing Streaming SIMD Extensions 2 (SSE2), Streaming SIMD Extensions 3 (SSE3) and Streaming SIMD Extensions 4 (SSE4). The processor supports several Advanced Technologies: Execute Disable Bit, Intel 64 Technology, Enhanced Intel SpeedStep Technology, Intel Virtualization Technology, and Simultaneous Multi Threading (SMT).

The following figure shows the Westmere-EP processor block diagram:

Figure 5-2 Nehalem/Westmere Processor block diagram



The following lists the main features of Westmere-EP processor used on ATCA-7368, L5638:

- Socket: LGA 1366
- Core Speed: 2.0GHz
- Cache Size
  - Instruction cache: 32Kb, per core
  - Data Cache: 32KB, per core
  - 256KB Mid-Level Cache (L2) per core
  - 12MB shared (L3) cache, running at core speed
- Data transfer rate: 2 full-width Intel QuickPath Interconnect links, 5.86GT/s in each direction
- Multi-core support: 6 core per processor
- Integrated memory controller, supporting DDR3 Memory speed, 800, 1066, 1333MHz
- Package: 1366 balls, FC-BGA
- TDP: 60W.

5.4 Memory

5.4.1 DDR3 Main Memory

ATCA-7368 provides a single Westmere-EP CPU with Integrated Memory Controller (IMC). IMC supports three independent 72-bit (64-bit Data + 8-bit ECC) wide DDR3 memory channels.

ATCA-7368 supports two VLP DIMM sockets for each memory channel resulting in a total of six DDR3 DIMM sockets.

Supported DDR3 speeds are DDR3-800 (PC3-6400), DDR3-1066 (PC3-8500), and DDR3-1333 (PC3-10600).

5.5 Chipset

The Xeon 5520 (Tylersburg IOH36 D) provides the interface between the processor Intel QuickPath Interconnect and industry-standard PCI Express components. The two Intel QuickPath Interconnect interfaces are full-width links (20 lanes in each direction). Xeon 5520 (Tylersburg IOH36 D) provides 36 PCI-e Gen2 Ports organized in three groups of 16, 16 and 4 PCI-e entities. The x16 PCIe Gen2 entities are also configurable as x8 and x4 links. In addition, the legacy Xeon 5520 (Tylersburg IOH36 D) supports an x4 ESI link interface (Enterprise South Bridge Interface) which connect to the Southbridge ICH10. The ESI is similar to an x4 PCI-express interface. The following figure gives an overview of the Xeon 5520 (Tylersburg IOH36 D) features.

5.6 I/O Controller

The ICH10R provides extensive I/O interface support and the boot path to SPI Boot Flash devices for the processor. ICH10R is connected to the system through the Enterprise Southbridge Interface (ESI) of the Xeon 5520 chipset.

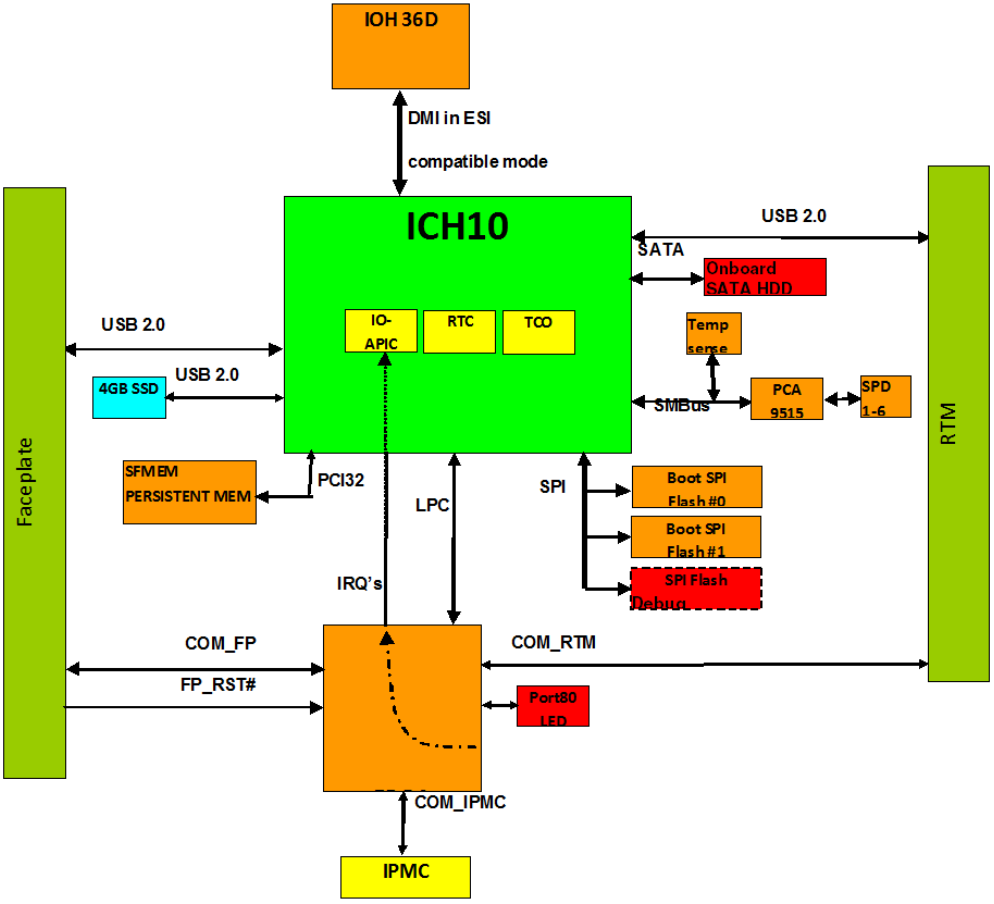
The following is a list of the main internal features and the I/O interface functions provided by the ICH10R Southbridge.

- Six x4 PCI Express 1.1 interface
- LPC interface
- SPI interface (Boot Flash): up to two devices 20 + 33 MHz
- Six serial ATA (SATA) interfaces
- Twelve USB 2.0 interfaces
- Two 8259 interrupt controllers and I/O APIC controllers
- Integrated I/O APIC
- Power management support
- Two 8237 DMA controller
- 8254-based Counter Timer/timers
- High-precision Event timers (HPET)
- RTC with 256-byte battery-backed SRAM

- System TCO (total cost of ownership) reduction circuits
- SMBus interface
- Two stage Watchdog timer
- PCI 2.3 interface 32-bit/ 33 MHz
- General purpose I/O pins

The following figure shows the I/O functions provided by ICH10R and those used on ATCA-7368:

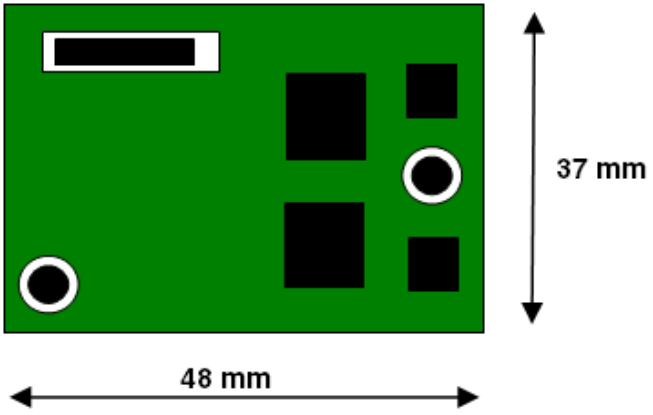
Figure 5-3 ICH10R Diagram



5.7 Persistent Memory Module (PMEM)

The ATCA-7368 provides a connector to assemble the Artesyn 7221-SFMEM (P/N #122265) module, a 48x37 low profile module integrating a PLX9030 PCI target-only Bridge and 64 Mb of Flash and 16 Mb of SRAM. The module connector is a 80-pin low density, low profile Molex Connector and features four configuration signals connected to the Glue Logic FPGA. Host and IPMC can configure the memory module through the configuration pins to use the FLASH as two 32 Mb mirrored banks (switchable, only one visible) or as continuous 64 MB Flash bank. Additionally, each bank is write protect able.

Figure 5-4 SFMEM-7221 Module dimensions (bottom view)



5.8 Ethernet Ports

The blade utilizes various Ethernet controllers that serve the ATCA Base I/F, Fabric I/F, Update Channel and Ethernet console. All Ethernet interfaces have 1GbE capability except for the Fabric I/F controller which can operate at 10 GbE or 1 GbE (PICMG 3.1 Option 9 and 1). The fabric I/F is fully operable in both 10G and 1G mode without the presence of an RTM.

Two Ethernet ports are available on the front panel. Additional Ethernet ports for external access are provided via the RTM.

The Ethernet controllers support I/O virtualization.

Table 5-1 Ethernet Controller Types

Interface	Location	Controller	Count	Ethernet Type
Base Interface	J6	Intel 82576	2 x	10,100,1G copper
Fabric Interface	J7	Intel 82599	2 x	10G/1G Serdes
Faceplate Interface	J402	Intel 82576	2 x	10,100,1 G Copper

5.9 Storage

ATCA-7368 supports the following types of storage:

- Onboard HDD/SSD with standard 2.5 inch form factor
- Onboard SATA Cube
- Persistent RAM module
- Onboard USB Flash (eUSB)
- Storage RTM with SATA/SAS support
- Storage AMC

5.10 IPMC

The blade features an Intelligent Platform Management Controller (IPMC) compliant to PICMG 3.0 and IPMI 1.5 and 2.0 (SOL only). The IPMC is a management subsystem providing monitoring, event logging, and recovery control. The IPMC serves as the gateway for management applications to access the payload hardware.

The IPMC firmware (FW) is stored in two independent memory images. Crisis recovery control is provided to allow reboot of the IPMC from a second image if the upgraded FW image is corrupted. FW images can be upgraded via HPM.1/IPMI using either IPMB or KCS interface.

The IPMC supports the initiation of a graceful shutdown of the host CPU. The IPMC can force the CPU to reset. It also controls the power and reset of the payload.

The IPMC provides a watchdog that supervises the payload. If enabled, the payload software needs to retrigger the Watchdog to prevent time-out. A watchdog time-out can generate a NMI, a payload reset or disabling/cycling of the payload power. The watchdog settings, including enable/disable, can be changed by payload software (setup menu). Time-out values can be selected from as short as seconds to as long as minutes.

The IPMC is supervised by a separate hardware Watchdog, which can not be disabled. IPMC FW retriggers the Watchdog timer.

The IPMC monitors the Port 80 POST codes generated by the payload CPU. The IPMC is connected to various sensors on the Blade that provide temperature sensor readings at all major devices and voltage sensor readings of all major voltages. The IPMC monitors reset events caused by devices like Watchdog, IPMI command, and reset button.

The FRU information of the various modules including front board, RTM, and other modules can be read via the IPMC and if necessary upgraded through the IPMC.

The IPMC features Serial over LAN (SOL) for the payload CPU serial console. The SOL interface is available via the ATCA Base I/F. SOL is activated by specific IPMI commands.

5.11 Serial Redirection

The CPU serial redirection reroutes the console input and output; that is the text output to the text screen and input from the standard keyboard. Typically, the console is used by the BIOS setup menus, BIOS initialization and boot routines, OS boot loaders and loaded OS.

The serial console of the payload CPU is available via SOL. In addition to the SOL capability, the serial console is also available on the blade faceplate using a RJ45 connector with Cisco pin-out. If a SOL session is established, only the output is available on the faceplate. Input is not possible during this time via the faceplate. Alternatively to the CPU serial console, the IPMC serial console is also available on the faceplate serial connector. It can be selected via specific IPMI OEM command.

5.12 Serial Over LAN

Serial Over LAN (SOL) enables suitably designed blades and servers to transparently redirect a serial character stream of a baseboard UART to/from a remote client via LAN over RMCP+ sessions. This enables users at remote consoles to access the serial port of a blade/server and interact with a text-based BIOS console, operating system, command line interfaces, and serial text-based applications.

The IPMC provides a dedicated sideband connection (SMBus) to the Base Interface Ethernet controller. Data from the payload serial redirection is routed thru the sideband connection to the Base I/F. Vice versa, the Ethernet controller filters packets based on either MAC address, RMCP port number, or IP address and forwards them to the serial redirection over the sideband interface.

Client software like openIPMI is required to enable SOL and to communicate with the SOL based serial console.

5.13 IPMI Over LAN

IPMI messages can be transferred over LAN (Base interface) using the RMCP protocol, as defined in the IPMI v1.5 specification, or using the RMCP+ protocol extension, as defined in the IPMI v2.0 specification. The RMCP/RMCP+ packets are formatted to contain IPMI request and response messages, plus additional messages for discovery and authentication.

The IPMI-over-LAN functionality is supported at a level that allows the Serial-over-LAN feature to be implemented.

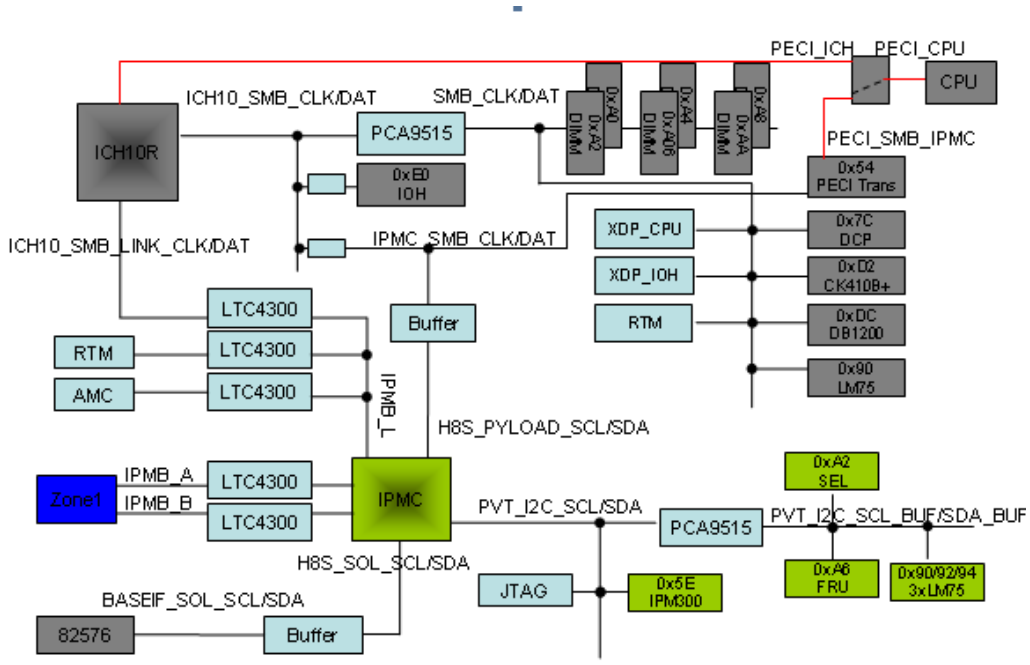
5.14 USB 2.0 Interface

The ICH10R provides internal USB1.1/ USB 2.0 host controllers with up to twelve USB 2.0 ports. Two ports are routed to the faceplate, one port is used onboard to connect a USB 2.0 SSD User Flash Module and one port is routed to the RTM. The ports available at the faceplate are routed to a dual stacked connector. The ports are USB 2.0 compliant.

5.15 SMBus Connections

The following figure shows the overall SMBus connections on ATCA-7368:

Figure 5-5 Overall SMBus Connections



The LM75 is a thermal sensor.

5.16 Real Time Clock

An external 32.768 kHz crystal sources the internal real time clock inside ICH10R with a frequency tolerance of 20 PPM. The RTC is fully-compliant with DS1287, MC14618, PC87911 and Y2K and provides 256 bytes of backed up CMOS RAM, of which 14 bytes containing the RTC time and date information, and RTC configuration. During power-down, the RTC consumes 0.9uA/hr. The optional power-down backup method uses a Super CAP with a 1 Farad capacity. This provides 300 hours of RTC/SRAM backup. The default battery is an external +3V lithium battery with a capacity of 200mAh, which provides three years of backup.

5.17 Single Width Mid-size AMC

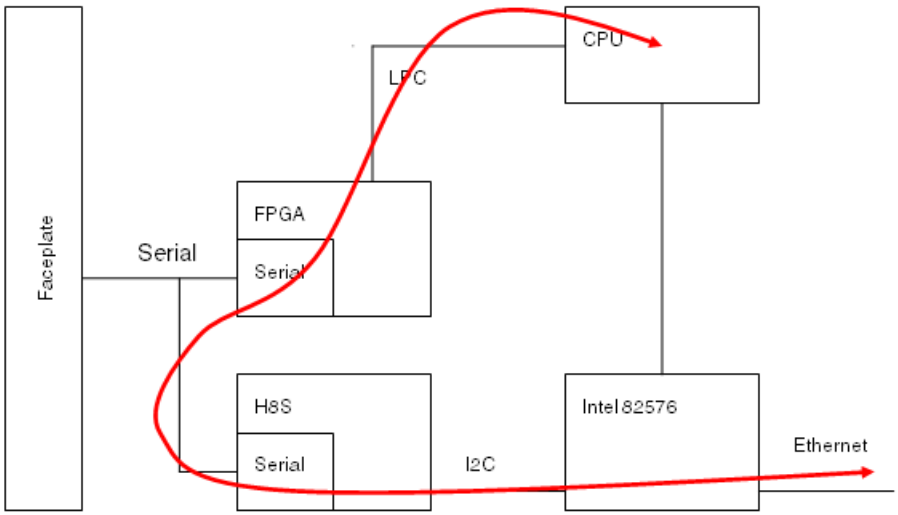
ATCA-7368 supports one slot of single width mid-size AMC to extend the application range of the blade by adding appropriate cards. This can be straight forward storage and network interface solutions or local storage hosted on an AMC. However it is also necessary to address applications requiring intelligent solutions that can handle tasks like TCP/IP off load, IPv4 and IPv6 stacks, unicast/multicast routing acceleration, IPSEC acceleration, firewall, SRTP offload, transport protocols, and mobile-IP, among others.

6.1 Overview

Serial Over LAN (SOL) is a mechanism that you can use to redirect the serial console from the blade via an IPMI session over the network. SOL uses the RMCP+ protocol.

The IPMC is used to establish and control the SOL session. SOL is only available on the base interface. The sideband interface of the Intel 82576 (in pass-through mode) is used to transmit/receive its terminal characters via the base interface.

Figure 6-1 SOL Overview



You can configure the SOL parameters using the standard IPMI commands or via an open source tool called "ipmitool".

6.2 Installing the ipmitool

You can download the open source tool ipmitool from http://ipmitool.sourceforge.net (at the time of publishing this manual the current version is 1.8.10). Documentation for this tool is also freely available on this site.

Procedure

To install the ipmitool, proceed as follows:

1. Download the ipmitool tar file from http://ipmitool.sourceforge.net to your blade.
2. Extract the source code.
   `prompt>tar -xjvf ipmitool-<version>.tar.bz2`
3. Go to the directory to which you have extracted the ipmitool.
   `prompt>cd <path>/ipmitool-<version>`
4. Build the ipmitool.
   `prompt>./configure && make && make install`

6.3 Configuring SOL Parameters

You can configure the following SOL parameters.

Table 6-1 SOL Parameters

Parameter	Description
Set LAN Configuration Parameter (IP address/MAC address)	Use this command to set the IP and MAC address.
Set Channel Access (Privilege level)	Use this command to set the privilege level.
Set User Name	Default value is soluser.
Set User Password	Default value is solpasswd.

You can use standard IPMI commands or the ipmitool to modify the parameters.

6.3.1 Using Standard IPMI Commands

This example shows how to set up the SOL configuration parameter with standard IPMI commands. Ipmicmd is used on the local IPMC and the IP is configured.

Sample Procedure

To set the IP address, proceed as follows:

1. Establish an IPMI connection to the blade.
2. Set LAN Configuration Parameter Set In Progress Lock.
   ipmicmd -k "f 0 c 1 5 0 1" smi 0
3. Set LAN Configuration Parameter Set IP (172.16.10.11 on channel 5).
   ipmicmd -k "f 0 c 1 5 3 ac 10 0a dd" smi 0
4. Set LAN Configuration Parameter Set In Progress Commit.
   ipmicmd -k "f 0 c 1 5 0 2" smi 0

6.3.2 Using ipmitool

The example below shows how to setup a LAN configuration parameter for a potential SOL session with ipmitool for base 1 (channel 5).

```
n0s70:~ #ipmitool lan set 5 ipaddr 172.16.0.221

Setting LAN IP Address to 172.16.0.221

n0s70:~ #
```

The following example shows how to query the LAN parameters that are currently in use for a potential SOL session for base 1 (channel 5) and base 2 (channel 6):

```
root@localhost:~# ipmitool lan print 5

Set in Progress         : Set Complete

Auth Type Support       :

Auth Type Enable        : Callback :

                        : User     :

                        : Operator :

                        : Admin    :
```

```
                          : OEM      :
IP Address Source         : Unspecified
IP Address                : 172.16.0.221
Subnet Mask               : 255.255.0.0
MAC Address               : 00:00:00:00:00:00
Default Gateway IP        : 172.16.0.1
Default Gateway MAC       : 00:00:00:00:00:00
RMCP+ Cipher Suites       : 1,2,3,3
Cipher Suite Priv Max     : Not Available
root@localhost:~# ipmitool lan print 6
Set in Progress           : Set Complete
Auth Type Support         :
Auth Type Enable          : Callback :
                          : User     :
                          : Operator :
                          : Admin    :
                          : OEM      :
IP Address Source         : Unspecified
IP Address                : 172.17.1.220
Subnet Mask               : 255.255.0.0
MAC Address               : 00:00:00:00:00:00
Default Gateway IP        : 172.17.0.1
Default Gateway MAC       : 00:00:00:00:00:00
```

```
RMCP+ Cipher Suites     : 1,2,3,3

Cipher Suite Priv Max   : Not Available

root@localhost:~#
```

MAC Address 00:00:00:00:00:00 means the address is shared between base and SOL interface. The address can be found out in the MAC address record of the FRU.

6.4 Establishing a SOL Session

To start a SOL session, the following requirements must be fulfilled:

- An Ethernet LAN connection to the 82576 controller of the ATCA-7368 must exist.
- ATCA-7368 IPMC FW must correspond to version 2.00.7 and above.

Procedure

To establish a SOL session, proceed as follows.:

1. Make sure that the requirements detailed above are fulfilled.
2. Compile and install the ipmitool on your target which is destined for opening the SOL session on the ATCA-7368. For details refer to *Installing the ipmitool* on page 97.
3. Apply an IP address to the ATCA-7368 SOL interface. For details refer to *Configuring SOL Parameters* on page 98.
4. If necessary change user and password.
   Default user is "soluser" and password is "solpasswd".
5. Configure the network between the ATCA-7368 and your target, which is destined for opening the SOL session, so that the SOL IP address is accessible.

6. Start ATCA-7368 SOL session on your target with the ipmitool and the configured IP address for the ATCA-7368 SOL interface.
   `ipmitool -C 1 -I lanplus -H 172.16.0.221 -U soluser -P solpasswd -k gkey sol activate`
   For details on the command parameters, refer to the ipmitool documentation available on http://ipmitool.sourceforge.net.

To access BIOS setup screen, it is necessary to reset the payload. SOL session is only available if the payload is powered on and initialized by the BIOS.

Supported IPMI Commands

7.1 Overview

This chapter describes the IPMI Commands supported on ATCA-7368.

7.2 Standard IPMI Commands

The IPMC is fully compliant to the Intelligent Platform Management Interface v.1.5. This section provides information about the supported IPMI commands.

7.2.1 Global IPMI Commands

The IPMC supports the following global IPMI commands.

Table 7-1 Supported Global IPMI Commands

Command	NetFn (Request/Response)	CMD	Comments
Get Device ID	0x06/0x07	0x01	-
Cold Reset	0x06/0x07	0x02	-
Warm Reset	0x06/0x07	0x03	-
Get Self Test Results	0x06/0x07	0x04	-
Get Device GUID	0x06/0x07	0x08	-
Master Write-Read	0x06/0x07	0x52	Only for accessing private I2C buses.

7.2.2 System Interface Commands

The watchdog commands are supported by blades providing a system interface and a watchdog type 2 sensor, also supported a OEM timeout action which is warm reset(04h).

Table 7-2 Supported System Interface Commands

Command	NetFn (Request/Response)	CMD
Set BMC Global Enables	0x06/0x07	0x2E
Get BMC Global Enables	0x06/0x07	0x2F
Clear Message Flags	0x06/0x07	0x30
Get Message Flags	0x06/0x07	0x31
Get Message	0x06/0x07	0x33
Send Message	0x06/0x07	0x34
Set Channel Access	0x06/0x07	0x40
Get Channel Access	0x06/0x07	0x41
Get Channel Info	0x06/0x07	0x42
Set User Access	0x06/0x07	0x43
Get User Access	0x06/0x07	0x44
Set User Name	0x06/0x07	0x45
Get User Name	0x06/0x07	0x46
Set User Password	0x06/0x07	0x47
Set User Payload Access	0x06/0x07	0x4C
Get User Payload Access	0x06/0x07	0x4D
Set Channel Security Keys	0x06/0x07	0x5C

7.2.3 Watchdog Commands

The watchdog commands are supported by blades providing a system interface and a watchdog type 2 sensor.

The options pre-timeout and power-cycle are not supported.

Table 7-3 Supported Watchdog Commands

Command	NetFn (Request/Response)	CMD
Reset Watchdog Timer	0x06/0x07	0x22
Set Watchdog Timer	0x06/0x07	0x24
Get Watchdog Timer	0x06/0x07	0x25

7.2.4 SEL Device Commands

Table 7-4 Supported SEL Device Commands

Command	NetFn (Request/Response)	CMD
Get SEL Info	0x0A/0x0B	0x40
Reserve SEL	0x0A/0x0B	0x42
Get SEL Entry	0x0A/0x0B	0x43
Add SEL Entry	0x0A/0x0B	0x44
Clear SEL	0x0A/0x0B	0x47
Get SEL Time	0x0A/0x0B	0x48
Set SEL Time	0x0A/0x0B	0x49

7.2.5 FRU Inventory Commands

Table 7-5 Supported FRU Inventory Commands

Command	NetFn (Request/Response)	CMD
Get FRU Inventory Area Info	0x0A/0x0B	0x10
Read FRU Data	0x0A/0x0B	0x11
Write FRU Data	0x0A/0x0B	0x12

7.2.6 Sensor Device Commands

Table 7-6 Supported Sensor Device Commands

Command	NetFn (Request/Response)	CMD	Comments
Get Device SDR Info	0x04/0x05	0x20	-
Get Device SDR	0x04/0x05	0x21	-
Reserve Device SDR Repository	0x04/0x05	0x22	-
Get Sensor Reading Factors	0x04/0x05	0x23	-
Set Sensor Hysteresis	0x04/0x05	0x24	-
Get Sensor Hysteresis	0x04/0x05	0x25	-
Set Sensor Threshold	0x04/0x05	0x26	Most of the threshold-based sensors have fixed thresholds. Before using this command, check whether threshold setting is supported by using the Get Device SDR command.
Get Sensor Threshold	0x04/0x05	0x27	-
Set Sensor Event Enable	0x04/0x05	0x28	-
Get Sensor Event Enable	0x04/0x05	0x29	-
Get Sensor Event Status	0x04/0x05	0x2B	-

Table 7-6 Supported Sensor Device Commands (continued)

Command	NetFn (Request/Response)	CMD	Comments
Get Sensor Reading	0x04/0x05	0x2D	-
Get Sensor Type	0x04/0x05	0x2F	-
Set Event Receiver	0x04/0x05	0x00	-
Get Event Receiver	0x04/0x05	0x01	-
Platform Event	0x04/0x05	0x02	-

7.2.7 Chassis Device Commands

Table 7-7 Supported Chassis Device Commands

Command	NetFn (Request/Response)	CMD
Set System Boot Options	0x00/0x01	0x08
Get System Boot Options	0x00/0x01	0x09

7.2.7.1 System Boot Options Commands

The IPMI system boot options commands allow you to control the boot process of a blade by sending boot parameters to the blade's boot firmware (for example BIOS, U-Boot or VxWorks). The boot firmware interprets the sent boot parameters and executes the boot process accordingly. Each boot parameter addresses a particular functionality and consists of a sequence of one or more bytes. The IPMI specification assigns numbers to boot parameters. Boot parameters 0 to 7 are standard parameters whose structure and functionality is defined by the IPMI specification. The boot parameters 96 to 127 are OEM-specific which can be used for different purposes.

When using the Get/Set System Boot Options commands, except for parameter 100, use the response/request data fields with the Set Selector and the Block Selector set to 0x00. When using the Get/Set System Boot Option for the parameter 100, the Set Selector and the Block Selector have a specific meaning. Details are given in *System Boot Options Parameter #100* on page 110 for details.

The following table lists which boot properties can be configured and the corresponding boot parameter number.

Table 7-8 Configurable System Boot Option Parameters

Configurable Boot Property	Corresponding Boot Parameter Number
Selection between default and backup boot flash as device to boot from Selection between default and backup EEPROM as device where the on-board FPGA loads its configuration stream from	96
POST Type	97
Timeout for graceful shutdown	98
BIOS boot parameters as defined in Table 7-15 on page 114	100

7.2.7.1.1 System Boot Options Parameter #96

This boot parameter is an Artesyn-specific OEM boot parameter. Its definition is given in the following table.

Table 7-9 System Boot Options Parameter #96

Data Byte	Description
1	Bits 7..1: Reserved Bit 0: Default/backup boot flash selection 0: Boot from default boot flash 1: Boot from backup boot flash Note: the newly selected boot flash is connected to the payload immediately, that means writing to the flash is possible. Its image is executed after the next power-up or cold reset of the payload.

The System Boot Options parameter #96 is non-volatile. During blade production, its data is initialized to 0xFF and its state is set to invalid. Its parameter data remains preserved after IPMC power cycles and firmware upgrades.

7.2.7.1.2 System Boot Options Parameter #97

This boot parameter is an Artesyn-specific OEM parameter. Its definition is given in the following table.

Table 7-10 System Boot Options Parameter #97

Data Byte	Description
1	POST Type Data 1 - Set Selector. This is the processor ID for which the boot option is to be set.
2	Data 2 - POST Type Selector. This parameter is used to specify the POST type that the IPMC will execute. 0x00: Short POST 0x01: Long POST 0x02 to 0xFF: Not used

The System Boot Options parameter #97 is non-volatile. During blade production, its data is initialized to 0xFF and its state is set to invalid. Its parameter data remains preserved after IPMC power cycles and firmware upgrades.

7.2.7.1.3 System Boot Options Parameter #98

This boot parameter is an Artesyn-specific OEM parameter.

This timer specifies how long the IPMC waits for the payload to shut down gracefully. If the payload software does not configure its OpenIPMI library to be notified for graceful shutdown requests, the IPMC shuts down the payload when the timer expires.

Table 7-11 System Boot Options Parameter #98

Bit	Description
15:8	Timeout for GRACEFUL_SHUTDOWN, LSB (given in 100 msec)
7:0	Timeout for GRACEFUL_SHUTDOWN, MSB (given in 100 msec)

The System Boot Options parameter #98 is non-volatile. During blade production its data is initialized to 0xFF and its state is set to invalid. Its parameter data remains preserved after IPMC power cycles and firmware upgrades.

7.2.7.1.4 System Boot Options Parameter #100

The system boot options parameter #100 allows you to send multiple boot options to the blade's boot firmware and thus control the boot process. The boot options which you can configure using this parameter are typically a subset of the boot options which you can configure in the boot firmware directly, for example, using a setup menu. Details are given in this section.

The IPMC contains a storage area where the boot parameters are stored. When the blade boots, the boot firmware reads out the storage area, interprets the parameters and executes the boot process accordingly. Note that the boot parameters in the IPMC storage area have higher priority than the same boot options which may be configured in the firmware itself, for example, using the setup menu.

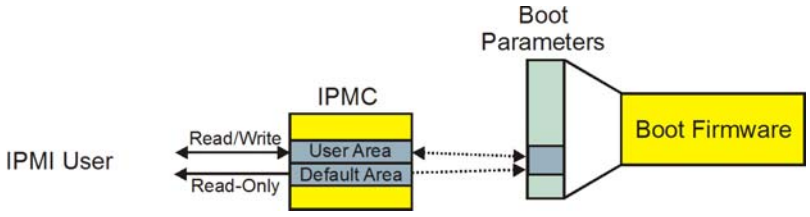
The storage area is divided into two parts: the default area and the user area. The user area can be read and written by an IPMI user and, by default, is the area which the boot firmware reads out and uses during the boot process. The default area can only be read (by both the IPMI user and the boot firmware.). Its purpose is to store factory-programmed default boot options which can be used to restore the standard settings. If you want the boot firmware to read out

and use the boot parameters stored in the default area and thus use the factory settings, you need to configure the blade accordingly. This is typically done by an on-board switch (for example, “Clear CMOS RAM”). It depends on the blade and firmware which settings are stored in the default area. Details are given in the following sections.

On some blades with particular firmware types, changing a boot parameter in the firmware setup menu changes the boot parameter in the user area as well, if the same parameter is defined both in the user area and the set-up menu. Details are given below.

The following figure summarizes the previously explained basic information flow related to the system boot options parameter #100.

Figure 7-1 System Boot Options Parameter #100 - Information Flow Overview



The boot options need to be stored as a sequence of zero terminated strings. The following table describes in detail the format of the boot options to be used when setting or reading the System Boot Options parameter #100.

Table 7-12 System Boot Options - Parameter #100 - Data Format

Byte	Description
0..1	Number of bytes used for boot parameters (LSB first) The number of bytes must be calculated and written into these two bytes by the software which writes into the storage area. The values 0x0000 and 0xFFFF indicate that no data has been written to the storage area. When reading from the storage area and you find any of these two values, your software should assume that no user-specific boot options have previously been written to the storage area.

Table 7-12 System Boot Options - Parameter #100 - Data Format (continued)

Byte	Description
2 .. n	Boot parameters data The boot parameters are stored as ASCII text with the following general format: <name>=<value>, where all name/value pairs are separated by a zero byte. The end of the boot parameter data is indicated by two zero bytes. Allowed and supported name/value pairs are blade-specific. Details are given below.
n + 1 .. n + 2	16 byte checksum over the boot parameters data section. (LSB first) For backward compatibility reasons, the checksums 0x0000 and 0xFFFF are accepted as valid. They indicate that no checksum has been calculated and stored.

When writing to or reading from the storage area, you can only read or write chunks of 16 bytes at a time. For this reason, the default and user area are divided into numbered blocks of 16 bytes which need to be addressed individually. For this purpose, the “Block Selector” field in the request data field is used. The “Set Selector” field, on the other hand, is used to select either the default or user area. The following two tables describe in detail how the request and response data fields need to be filled and interpreted when performing SET and GET accesses.

Table 7-13 System Boot Options Parameter #100 - SET Command Usage

Byte	Description
Request Data	
1	Bit 7: when set to "1", the storage area on the IPMC is locked, i.e. no other software can access it. This should be set, before doing any modifications and cleared again after the final access. Bits 6..0: must contain the value: "100" indicating this OEM system boot option.
2	Set Selector Must be set to "0" (user area). You can only write to the user area, therefore no other values are supported.
3	Block Selector Zero based index of the 16-byte block which you want to write to. Index 0 refers to the first block of 16 bytes, which includes the first two bytes that indicate the boot parameter data size. Depending on the total length of the boot option data, your software may need to write several blocks of 16 bytes in a row, each individually addressed using the block selector.

Table 7-13 System Boot Options Parameter #100 - SET Command Usage (continued)

Byte	Description
4 .. n (n <= 19)	Data that you want to write into the addressed block. This will be a chunk of the boot parameter data. If less than 16 bytes are written, then only the provided data is written, the remaining bytes in the addressed storage area block are left unchanged.
Response Data	
1	0x00: Write successful 0x80: Boot parameter storage not supported by the IPMC 0x81: Storage area is locked by another software entity 0x82: Illegal write-access 0xC9: Block selector is outside of the allowed range.

Table 7-14 System Boot Options Parameter #100 - GET Command Usage

Byte	Description
Request Data	
1	Bit 7: reserved. Set to "0". Bits 6..0: must contain the value:" 100", indicating this OEM system boot option.
2	Set Selector 0: User area 1: Default area
3	Block Selector Zero based index of the 16-byte block which you want to read from. Index 0 refers to the first block of 16 bytes, which includes the first two bytes which indicate the boot parameter data size.
Response Data	
1	0x00: Read successful 0x80: Boot parameter storage not supported by the IPMC 0xC9: Block selector is outside of the allowed range.
2	Reserved. Set to "1".
3	Bit 7: If set to "1", the addressed storage area is locked. Bits 6 ..0: value "100", indicating this OEM boot option command.

Table 7-14 System Boot Options Parameter #100 - GET Command Usage (continued)

Byte	Description
4 .. 19	The content of the read 16-byte block.

In order to detect the maximum size of writable storage area, your software can perform a series of read accesses while incrementing the block selector with each access. Once the error code C9 is returned, the limit has been reached and the total available space in the writable storage area can be easily determined by the number of previously performed successful read accesses.

This is supported by HPI, for details refer to the *System Management Interface Based on HPI-B User's Guide* related to your system environment.

The following table lists boot parameters which can be configured for the ATCA-7368 blade, using the system boot option parameter #100.

Artesyn provides the tool "ipmibpar" to interpret the ASCII parameters. To obtain the tool, contact your local sales representative.

When used in the System Boot Options parameter #100, the boot parameters and their values are case-sensitive.

All boot options listed in the following table are set by the BIOS setup menu and can be configured using the System Boot options command #100. The IPMC and BIOS software automatically synchronize the settings made in the BIOS setup menu and the settings specified using the System Boot Options command #100. Changing a parameter in either of these, automatically changes the respective value in the other.

Table 7-15 System Boot Options Parameter #100 - Supported Parameters

Parameter	Options	Default Values
proc_o_speed	1.5:1.7?1.8?2.0	2.0
ecc_support	on:off	on
hyper_threading	on:off	on
act_core	all:1:2:3:4:5	all

Table 7-15 System Boot Options Parameter #100 - Supported Parameters (continued)

Parameter	Options	Default Values
limit_cpuid	on:off	on
hw_prefetcher	on:off	on
adj_cache_prefetch	on:off	on
virtualization	on:off	on
turbo_mode	on:off	on
rt_err_log	on:off	on
err_threshold	1:10:15	10
vt_d	on:off	off
int_map	on:off	on
qpi_freq_sel	auto:4.8:5.8:6.4	auto
mem_mode	ind:mir:lst:spr	ind
ch_interleave	auto:6:4:3:2:1	auto
rank_interleave	auto:4:2:1	auto
hw_mem_test	on:off	on
patrol_scrub	on:off	on
demand_scrub	on:off	off
all_usb_device	on:off	on
usb_2.0_cont_mode	on:off	on
usb	fp_on:fp_off	fp_on
	rtm_on:rtm_off	rtm_on
	onboard_on:onboard_off	onboard_on
usb_boot	on:off	on
sata_mode	off:ide:ahci:raid	ide
sata_cont_0	off:enhc:cmpt	cmpt
sata_cont_1	off:enhc:cmpt	enhc
ehci_hand_off	on:off	on
dev_reset_time	10:20:30:40	20

Table 7-15 System Boot Options Parameter #100 - Supported Parameters (continued)

Parameter	Options	Default Values
com1	on:off	on
com1_setting	auto:3f8_4:3f8_a:2f8_a:3e8_a:2e8_a	3f8_4
com_cr	on:off	on
term_type	vt100: vt100+: vt-utf8: ansi	vt100
baudrate	9600: 19200: 38400: 57600: 115200	9600
data_bits	7:8	8
parity	none:even:odd:mark:space	none
stop_bits	1:2	1
os_boot_watchdog	on:off	off
	1:2:3:5:7:10:15:20	5
	nothing:reset:pwdw:pwcy	reset
bios_watchdog	on:off	on
	3:4:5:6	3
	reset	reset
log_status_code	off:both:errcode:prgcode	both
frontnet_boot	on:off	off
basenet_boot	on:off	on
fabricnet_boot	on:off	off
artm_net_boot	on:off	off
artm_sas_boot	on:off	on
ssc_support	on:off	on
wait_rtm_time	numeric(0~255)	0
wait_rtm_policy	force:auto	auto
setup_timeout	numeric(0~65535)	4
number_lock	on:off	on
pci_err_log	on:off	on

Table 7-15 System Boot Options Parameter #100 - Supported Parameters (continued)

Parameter	Options	Default Values
err_threshold	numeric(1~1000)	10
err_log_limit	numeric(1~20)	10
Config_iou1	44:48:84:88:16	44
Transf_timeout	1:5:10:20	20
powerup_delay	auto:manual	auto
flow_ctrl	none:hwrc:swct	none
erase_event_log	no:next:every	no
act_log_full	nothing:erase	nothing
Boot_order	device1,devcice2,..device8 See Table 7-16	

Table 7-16 boot_order Devices

Device	Description
sata0	SATA device 0 (Debug SATA)
sata1	SATA device 1 (RTM Debug SATA)
sata5	SATA device 5 (Onboard SATA)
sataonboard	SATA device 5 (Onboard SATA)
sashdd	SAS HDD mounted on the RTM
sas0_nn	SAS Controller nn = SCSI ID (use this when a SAS array is connected to the RTM)
frontnet	Front Panel Network
basenet0	Base0 Network
basenet1	Base1 Network
usb1	USB frontpanel 1
usb2	USB frontpanel 2
usbonboard	USB onboard HDD
usbartm	USB artm
usbkey	USB key

Table 7-16 boot_order Devices (continued)

Device	Description
usbcdrom	USB cdrom
usbhdd	USB hdd
usbfdd	USB floppy disk
efishell	Built in UEFI shell
Up to 8 boot devices are supported. Example: boot_order=sas0_03,basenet0,usbkey,sata1	

7.2.8 LAN Device Commands

Table 7-17 Supported LAN Device Commands

Command	NetFn (Request/Response)	CMD
Set LAN Configuration Parameters	0x0C/0x0D	0x01
Get LAN Configuration Parameters	0x0C/0x0D	0x02
Set SOL Configuration Parameters	0x0C/0x0D	0x21
Get SOL Configuration Parameters	0x0C/0x0D	0x22

7.3 PICMG 3.0 Commands

The Artesyn Embedded Technologies IPMC is a fully compliant AdvancedTCA intelligent Platform Management Controller.It supports all required and mandatory AdvancedTCA commands as defined in the PICMG 3.0 and AMC.0 R2.0 specifications.

Table 7-18 Supported PICMG 3.0 Commands

Command	NetFn (Request/Response)	CMD	Comments
Get PICMG Properties	0x2C/0x2D	0x00	-
Get Address Info	0x2C/0x2D	0x01	-
FRU Control	0x2C/0x2D	0x04	-
Get FRU LED Properties	0x2C/0x2D	0x05	-
Get FRU LED Color Capabilities	0x2C/0x2D	0x06	-
Set FRU LED State	0x2C/0x2D	0x07	-
Get FRU LED State	0x2C/0x2D	0x08	-
Set IPMB State	0x2C/0x2D	0x09	-
Set FRU Activation Policy	0x2C/0x2D	0x0A	-
Get FRU Activation Policy	0x2C/0x2D	0x0B	-
Set FRU Activation	0x2C/0x2D	0x0C	-
Get Device Locator Record ID	0x2C/0x2D	0x0D	The Artesyn Embedded Technologies IPMCs support the standard PICMG 3.0 and the extended AMC.0 R2.0 versions of this command.
Set Port State	0x2C/0x2D	0x0E	-
Get Port State	0x2C/0x2D	0x0F	-
Compute Power Properties	0x2C/0x2D	0x10	-
Set Power Level	0x2C/0x2D	0x11	-
Get Power Level	0x2C/0x2D	0x12	-
Get IPMB Link Info	0x2C/0x2D	0x18	-

Table 7-18 Supported PICMG 3.0 Commands (continued)

Command	NetFn (Request/Response)	CMD	Comments
Set AMC Port State	0x2C/0x2D	0x19	-
Get AMC Port State	0x2C/0x2D	0x1A	-
Get FRU Control Capabilities	0x2C/0x2D	0x1E	-
Get target upgrade capabilities	0x2C/0x2D	0x2E	-
Get component properties	0x2C/0x2D	0x2F	-
Abort firmware upgrade	0x2C/0x2D	0x30	-
Initiate upgrade action	0x2C/0x2D	0x31	-
Upload firmware block	0x2C/0x2D	0x32	-
Finish firmware upload	0x2C/0x2D	0x33	-
Get upgrade status	0x2C/0x2D	0x34	-
Activate firmware	0x2C/0x2D	0x35	-
Query self-test results	0x2C/0x2D	0x36	-
Query rollback status	0x2C/0x2D	0x37	-
Initiate manual rollback	0x2C/0x2D	0x38	-

The firmware upgrade commands supported by the blade are implemented according to the PICMG HPM.1 Revision 1.0 specification.

The boot block can be updated with PICMG HPM.1 specific commands.

7.4 Artesyn Specific Commands

The Artesyn IPMC supports several commands which are not defined in the IPMI or PICMG 3.0 specification but are introduced by Artesyn Embedded Technologies: serial output commands.

- Before sending any of these commands, the shelf management software must check whether the receiving IPMI controller supports Artesyn specific IPMI commands by using the IPMI command 'Get Device ID'. Sending Artesyn specific commands to IPMI controllers which do not support these IPMI commands will lead to no or undefined results.
- Proper handling of these commands is required to write a portable application.

7.4.1 Set/Get Feature Configuration

This command can be used to enable/disable features within the IPMC during runtime.

Table 7-19 Set/Get Feature Configuration

Command Name	NetFn (Request/Response)	CMD	Description
Set Feature Configuration	0x2E/0x2F	0x1E	
Get Feature Configuration	0x2E/0x2F	0x1F	

7.4.1.1 Set Feature Configuration (0x1E)

This command can be used to set the IPMI feature.

Table 7-20 Set Feature Configuration Command

	Byte	Data Field
Request Data	1	LSB of Artesyn IANA Enterprise Number. A value of CDh shall be used.
	2	2nd byte of Artesyn IANA Enterprise Number. A value of 65h shall be used.
	3	MSB of Artesyn IANA Enterprise Number. A value of 00h shall be used.
	4	Feature Selector. For details, please see Table 2-16 Feature Selector Assignments
	5	Feature Configuration 00h = disabled (Feature Selector = E2h) 01h = enabled (Feature Selector = E2h)-Default 02h - FFh = reserved
	6	Persistency / Duration 00h = volatile. Actual duration depends on implementation. 01h - FFh = reserved
Response Data	1	Completion Code. Generic plus the following command-specific completion codes: 80h = feature selector not supported. 81h = feature configuration not supported 82h = configuration persistency / duration not supported
	2	LSB of Artesyn IANA Enterprise Number. A value of CDh shall be used.
	3	2nd byte of Artesyn IANA Enterprise Number. A value of 65h shall be used.
	4	MSB of Artesyn IANA Enterprise Number. A value of 00h shall be used.

Table 7-21 Feature Selector Assignments

Feature Selector	Description
E2h	Boot Firmware Automatic Switchover Function Enable/Disable

7.4.1.2 Get Feature Configuration (0x1F)

This command can be used to retrieve the IPMI feature set being configured.

Table 7-22 Get Feature Configuration Command

	Byte	Data Field
Request Data	1	LSB of Artesyn IANA Enterprise Number. A value of CDh shall be used.
	2	2nd byte of Artesyn IANA Enterprise Number. A value of 65h shall be used.
	3	MSB of Artesyn IANA Enterprise Number. A value of 00h shall be used.
	4	Feature Selector, for details see Table 7-23 on page 124.
Response Data	1	Completion Code. Generic plus the following command-specific completion codes: 80h = feature selector not supported.
	2	LSB of Artesyn IANA Enterprise Number. A value of CDh shall be used.
	3	2nd byte of Artesyn IANA Enterprise Number. A value of 65h shall be used.
	4	MSB of Artesyn IANA Enterprise Number. A value of 00h shall be used.
	5	Feature Configuration
	6	Persistency / Duration

Table 7-23 Feature Selector Assignments

Feature Selector	Description
E2h	Boot Firmware Automatic Switchover Function Enable/Disable

7.4.2 Serial Output Commands

Table 7-24 Serial Output Commands

Command Name	NetFn (Request/Response)	CMD	Description
Set Serial Output	0x2E/0x2F	0x15	See *Set Serial Output Command* on page 124
Get Serial Output	0x2E/0x2F	0x16	See *Get Serial Output Command* on page 125

7.4.2.1 Set Serial Output Command

The Set Serial Output command selects the serial port output source for a serial port connector.

7.4.2.1.1 Request Data

The following table lists the request data applicable to the Set Serial Output command.

Table 7-25 Request Data of Set Serial Output Command

Byte	Data Field
1	LSB of Artesyn Embedded Technologies IANA Enterprise number. A value of 0xCD has to be used.
2	Second byte of Artesyn Embedded Technologies IANA Enterprise number. A value of 0x65 has to be used.
3	MSB of Artesyn Embedded Technologies IANA Enterprise number. A value of 0x00 has to be used.

Table 7-25 Request Data of Set Serial Output Command (continued)

Byte	Data Field
4	Serial connector type 0: faceplate connector 1: Backplane connector All other values are reserved. Note: Only the faceplate connector is supported. No connector on the RTM available.
5	Serial connector instance number. A sequential number that starts from "0".
6	Serial output selector 0: BIOS 2: IPMC debug console All other values are reserved.

7.4.2.1.2 Response Data

The following table lists the response data applicable to the Set Serial Output command.

Table 7-26 Response Data of Set Serial Output Command

Byte	Data Field
1	Completion code
2	LSB of Artesyn Embedded Technologies IANA Enterprise number.
3	Second byte of Artesyn Embedded Technologies IANA Enterprise number.
4	MSB of Artesyn Embedded Technologies IANA Enterprise number.

7.4.2.2 Get Serial Output Command

The Get Serial Output Command provides a way to determine which serial output source goes to a particular serial port connector.

Currently, only BIOS output is supported.

7.4.2.2.1 Request Data

The following table lists the request data applicable to the Get Serial Output command.

Table 7-27 Request Data of Get Serial Output Command

Byte	Data Field
1	LSB of Artesyn IANA Enterprise number. A value of 0xCD has to be used.
2	Second byte of Artesyn IANA Enterprise number. A value of 0x65 has to be used.
3	MSB of Artesyn Embedded Technologies IANA Enterprise number. A value of 0x00 has to be used.
4	Serial connector type 0: faceplate connector 1: Backplane connector All other values are reserved. Note: Only the faceplate connector is supported. No connector on the RTM available.
5	Serial connector instance number. A sequential number that starts from "0".

7.4.2.2.2 Response Data

The following table lists the response data applicable to the Get Serial Output command.

Table 7-28 Response Data of Get Serial Output Command

Byte	Data Field
1	Completion code
2	LSB of Artesyn Embedded Technologies IANA Enterprise number.
3	Second byte of Artesyn Embedded Technologies IANA Enterprise number.
4	MSB of Artesyn Embedded Technologies IANA Enterprise number.
5	Serial output selector

7.5 Pigeon Point Specific Commands

The IPMC supports additional IPMI commands that are specific to Pigeon Point. This section provides detailed descriptions of those extensions:

Table 7-29 Pigeon Point Extension Commands

Command	NetFn (Request/Response)	CMD
Get Status Table 7-31 on page 128	0x2E/0x2F	0x00
Get Serial Interface Properties Table 7-32 on page 131	0x2E/0x2F	0x01
Set Serial Interface Properties Table 7-33 on page 132	0x2E/0x2F	0x02
Get Debug Level Table 7-34 on page 133	0x2E/0x2F	0x03
Set Debug Level Table 7-35 on page 134	0x2E/0x2F	0x04
Get Hardware Address Table 7-36 on page 135	0x2E/0x2F	0x05
Set Hardware Address Table 7-37 on page 135	0x2E/0x2F	0x06
Get Handle Switch Table 7-38 on page 136	0x2E/0x2F	0x07
Set Handle Switch Table 7-39 on page 137	0x2E/0x2F	0x08
Get Payload Communication Time-Out Table 7-40 on page 137	0x2E/0x2F	0x09
Set Payload Communication Time-Out Table 7-41 on page 138	0x2E/0x2F	0x0A
Enable Payload Control Table 7-42 on page 139	0x2E/0x2F	0x0B
Disable Payload Control Table 7-43 on page 139	0x2E/0x2F	0x0C
Reset IPMC Table 7-44 on page 140	0x2E/0x2F	0x0D
Hang IPMC Table 7-45 on page 140	0x2E/0x2F	0x0E
Graceful Reset Table 7-46 on page 141	0x2E/0x2F	0x11
Get Payload Shutdown Time-Out Table 7-47 on page 142	0x2E/0x2F	0x15
Set Payload Shutdown Time-Out Table 7-48 on page 143	0x2E/0x2F	0x16
Get Module State Table 7-49 on page 143	0x2E/0x2F	0x27
Enable Module Site Table 7-50 on page 145	0x2E/0x2F	0x28
Disable Module Site Table 7-51 on page 145	0x2E/0x2F	0x29

Table 7-29 Pigeon Point Extension Commands (continued)

Command	NetFn (Request/Response)	CMD
Reset Carrier SDR repository Table 7-52 on page 146	0x2E/0x2F	0x33

Some of the following commands refer to IPMC modes which are defined as follows:

Table 7-30 IPMC Modes

Mode	Description
Standalone	In standalone mode, the carrier IPMC disconnects from IPMB-0 but keeps on listening to the serial debug and payload interfaces and serving requests coming from them, as well as managing the modules, AMC point-to-point (P2P) and clock E-keying. Standalone mode is intended for debugging purposes and/or operation in a non-ATCA environment. In standalone mode, the carrier IPMC automatically activates and deactivates the on-carrier payload and modules whenever it does not violate any carrier limitations.
Manual standalone	Manual standalone mode is equivalent to standalone mode with only one exception: carrier IPMC control over the on-carrier payload is automatically disabled in manual standalone mode.

7.5.1 Get Status Command

The Get Status command can be used by the payload software to retrieve the status of the IPMC.

Table 7-31 Get Status Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

Table 7-31 Get Status Command Description (continued)

Type	Byte	Data Field
	5	Bit [7] Graceful Reboot Request If set to "1", indicates that the payload is requested to initiate the graceful reboot sequence. Bit [6] Diagnostic Interrupt Request If set to "1", indicates that a payload diagnostic interrupt request has arrived. Bit [5] Shutdown Alert If set to "1", indicates that the payload is going to be shutdown. Bit [4] Reset Alert If set to "1", indicates that the payload is going to be reset. Bit [3] Sensor Alert If set to "1", indicates that at least one of the IPMC sensors detects a threshold crossing. Bits [2:1] Mode The current IPMC modes are defined as: 0: Normal 1: Standalone, for a description refer to Table 7-30 2: Manual Standalone, for a description refer to Table 7-30 Bit [0] Control If set to 0, the IPMC control over the payload is disabled.
	6	Bits [4:7] Metallic Bus 2 Events These bits indicate pending Metallic Bus 2 requests arrived from the shelf manager: 0: Metallic Bus 2 Query 1: Metallic Bus 2 Release 2: Metallic Bus 2 Force 3: Metallic Bus 2 Free Bits [0:3] Metallic Bus 1 Events These bits indicate pending Metallic Bus 1 requests arrived from the shelf manager: 0: Metallic Bus 1 Query 1: Metallic Bus 1 Release 2: Metallic Bus 1 Force 3: Metallic Bus 1 Free

Table 7-31 Get Status Command Description (continued)

Type	Byte	Data Field
	7	Bits [4:7] Clock Bus 2 Events These bits indicate pending Clock Bus 2 requests arrived from the shelf manager: 0: Clock Bus 2 Query 1: Clock Bus 2 Release 2: Clock Bus 2 Force 3: Clock Bus 2 Free Bits [0:3] Clock Bus 1 Events These bits indicate pending Clock Bus 1 requests arrived from the shelf manager: 0: Clock Bus 1 Query 1: Clock Bus 1 Release 2: Clock Bus 1 Force 3: Clock Bus 1 Free
	8	Bits [4:7] Reserved Bits [0:3] Clock Bus 3 Events These bits indicate pending Clock Bus 3 requests arrived from the shelf manager: 0: Clock Bus 3 Query 1: Clock Bus 3 Release 2: Clock Bus 3 Force 3: Clock Bus 3 Free

7.5.2 Get Serial Interface Properties Command

The Get Serial Interface Properties command is used to get the properties of a particular serial interface.

Table 7-32 Get Serial Interface Properties Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Interface ID 0: Serial Debug Interface
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00
	5	Bit [7] Echo On If this bit is set, the IPMC enables echo for the given serial interface. Bits [6:4] Reserved Bits [3:0] Baud Rate ID The baud rate ID defines the interface baud rate as follows: 0: 9600 bps 1: 19200 bps 2: 38400 bps 3: 57600 bps (unsupported) 4: 115200 bps (unsupported)

7.5.3 Set Serial Interface Properties Command

The Set Serial Interface Properties command is used to set the properties of a particular serial interface.

Table 7-33 Set Serial Interface Properties Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Interface ID 0: Serial Debug Interface
	5	Bit [7] Echo On If this bit is set, the IPMC enables echo for the given serial interface. Bits [6:4] Reserved Bits [3:0] Baud Rate ID The baud rate ID defines the interface baud rate as follows: 0: 9600 bps 1: 19200 bps 2: 38400 bps 3: 57600 bps (unsupported) 4: 115200 bps (unsupported)
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

7.5.4 Get Debug Level Command

The Get Debug Level command gets the current debug level of the IPMC firmware.

Table 7-34 Get Debug Level Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00
	5	Bit [7] IPMB-L Dump Enable If set to 1, the IPMC provides a trace of IPMB-L messages that are arriving to/going from the IPMC via IPMB-L. Bit [6] n/a Bit [5] KCS Dump Enable If set to "1", the IPMC provides a trace of KCS messages that are arriving to/going from the IPMC via KCS. Bit [4] IPMB Dump Enable If set to "1", the IPMC provides a trace of IPMB messages that are arriving to/going from the IPMC via IPMB-O. Bit [3] n/a Bit [2] Alert Logging Enable If set to "1", the IPMC outputs important alert messages onto the serial debug interface. Bit [1] Low-level Error Logging Enable If set to "1", the IPMC outputs low-level error/diagnostic messages onto the serial debug interface. Bit [0] Error Logging Enable If set to "1", the IPMC outputs error/diagnostic messages onto the serial debug interface.

7.5.5 Set Debug Level Command

The Set Debug Level command sets the current debug level of the IPMC firmware.

Table 7-35 Set Debug Level Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Bit [7] IPMB-L Dump Enable If set to "1", the IPMC provides a trace of IPMB-L messages that are arriving to/going from the IPMC via IPMB-L. Bit [6] n/a Bit [5] KCS Dump Enable If set to "1", the IPMC provides a trace of KCS messages that are arriving to/going from the IPMC via KCS. Bit [4] IPMB Dump Enable If set to "1", the IPMC provides a trace of IPMB messages that are arriving to/going from the IPMC via IPMB-O. Bit [3] n/a Bit [2] Alert Logging Enable If set to "1", the IPMC outputs important alert messages onto the serial debug interface. Bit [1] Low-level Error Logging Enable If set to "1", the IPMC outputs low-level error/diagnostic messages onto the serial debug interface. Bit [0] Error Logging Enable If set to "1", the IPMC outputs error/diagnostic messages onto the serial debug interface.
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

7.5.6 Get Hardware Address Command

The Get Hardware Address command reads the hardware address of the IPMC.

Table 7-36 Get Hardware Address Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00
	5	Hardware Address

7.5.7 Set Hardware Address Command

The Set Hardware Address command allows the user to override the hardware address read from the hardware when the IPMC operates in (manual) standalone mode (for a description refer to Table 7-30).

Table 7-37 Set Hardware Address Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Hardware Address If set to 00, the ability to override the hardware address is disabled. NOTE: A hardware address change only takes effect after an IPMC reset.
Response Data	1	Completion Code

Table 7-37 Set Hardware Address Command Description (continued)

Type	Byte	Data Field
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

7.5.8 Get Handle Switch Command

The Get Handle Switch command reads the state of the hot-swap handle of the IPMC. Overriding of the handle switch state is allowed only if the IPMC operates in (manual) standalone mode (for a description refer to Table 7-30).

Table 7-38 Get Handle Switch Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	FRU ID (specify as 0)
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00
	5	Handle Switch Status 0x00: The handle switch is open. 0x01: The handle switch is closed. 0x02: The handle switch state is read from hardware.

7.5.9 Set Handle Switch Command

The Set Handle Switch command sets the state of the hot-swap handle switch in (manual) standalone mode (for a description refer to Table 7-30).

Table 7-39 Set Handle Switch Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	FRU ID (specify as 0)
	5	Handle Switch Status 0x00: The handle switch is open. 0x01: The handle switch is closed. 0x02: The handle switch state is read from hardware.
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

7.5.10 Get Payload Communication Time-Out Command

The Get Payload Communication Time-Out command reads the payload communication time-out value.

Table 7-40 Get Payload Communication Time-Out Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code

Table 7-40 Get Payload Communication Time-Out Command Description (continued)

Type	Byte	Data Field
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00
	5	Payload Time-out Payload communication time-out measured in hundreds of milliseconds. Thus, the payload communication time-out may vary from 0.1 to 25.5 seconds.

7.5.11 Set Payload Communication Time-Out Command

The Set Payload Communication Time-Out command sets the payload communication time-out value.

Table 7-41 Set Payload Communication Time-Out Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Payload Time-out Payload communication time-out measured in hundreds of milliseconds. Thus, the payload communication time-out may vary from 0.1 to 25.5 seconds.
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

7.5.12 Enable Payload Control Command

The Enable Payload Control command enables payload control from the serial debug interface.

Table 7-42 Enable Payload Control Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

7.5.13 Disable Payload Control Command

The Disable Payload Control command disables payload control from the serial debug interface.

Table 7-43 Disable Payload Control Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

7.5.14 Reset IPMC Command

The Reset IPMC command allows the payload to reset the IPMC over the KCS host interface.

Table 7-44 Reset IPMC Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Reset Type Code 0x00: Cold IPMC reset to the current mode 0x01: Cold IPMC reset to the Normal mode 0x02: Cold IPMC reset to the Standalone mode, for a description refer to Table 7-30 0x03: Cold IPMC reset to the Manual Standalone mode, for a description refer to Table 7-30 0x04: Reset the IPMC and enter Upgrade mode
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

7.5.15 Hang IPMC Command

The IPMC provides a way to test the watchdog timer support by implementing the Hang IPMC command, which simulates firmware hanging by entering an endless loop.

Table 7-45 Hang IPMC Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code

Table 7-45 Hang IPMC Command Description (continued)

Type	Byte	Data Field
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

7.5.16 Graceful Reset Command

The IPMC supports the Graceful Reboot option of the FRU Control command. On receiving such a command, the IPMC sets the Graceful Reboot Request bit of the IPMC status, sends a status update notification to the payload, and waits for the Graceful Reset command from the payload. If the IPMC receives such a command before the payload communication time-out time, it sends the 0x00 completion code (Success) to the shelf manager. Otherwise, the 0xCC completion code is sent.

The IPMC does not reset the payload upon receiving the Graceful Reset command or time-out. If the IPMC participation is necessary, the payload must request the IPMC to perform a payload reset. The Graceful Reset command is also used to notify the IPMC about the completion of the payload shutdown sequence.

Table 7-46 Graceful Reset Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

7.5.17 Get Payload Shutdown Time-Out Command

When the shelf manager commands the IPMC to shut down the payload (i.e. sends the Activate FRU (Deactivate) command), the IPMC notifies the payload by forwarding the command Activate FRU (Deactivate) to the KCS interface. Provided the OpenIPMI driver has registered this command for notification, the payload gets notified. Upon receiving this notification, the payload software is expected to initiate the payload shutdown sequence. After performing this sequence, the payload should send the Graceful Reset command to the IPMC over the payload Interface to notify the IPMC that the payload shutdown is complete.

To avoid deadlocks that may occur if the payload software does not respond, the IPMC provides a special time-out for the payload shutdown sequence. If the payload does not send the Graceful Reset command within a definite period of time, the IPMC assumes that the payload shutdown sequence is finished, and resets the payload.

Table 7-47 Get Payload Shutdown Time-Out Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00
	5:6	Time-Out measured in hundreds of milliseconds, LSB first

7.5.18 Set Payload Shutdown Time-Out Command

The Set Payload Shutdown Time-Out command is defined as follows.

Table 7-48 Set Payload Shutdown Time-Out Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4:5	Time-Out measured in hundreds of milliseconds, LSB first
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

7.5.19 Get Module State Command

The Get Module State command is used to query the state of a module (RTM with site ID1) using any of the external interfaces.

Table 7-49 Get Module State Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Module Site ID
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

Table 7-49 Get Module State Command Description (continued)

Type	Byte	Data Field
	5	Module Status Bit [0] 0: Module site is enabled. 1: Module site is disabled. Bit [1] 0: Module is not present. 1: Module is present. Bit [2] 0: Management power is disabled. 1: Management power is enabled. Bit [3] 0: Management power is bad. 1: Management power is good. Bit [4] 0: Payload power is disabled. 1: Payload power is enabled. Bit [5] 0: Payload power is bad. 1: Payload power is good. Bit [6] 0: IPMB-L buffer is not attached. 1: IPMB-L buffer is attached. Bit [7] 0: IPMB-L buffer is not ready. 1: IPMB-L buffer is ready.

7.5.20 Enable Module Site Command

The Enable Module Site command is used to enable a module site.

Table 7-50 Enable Module Site Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Module Site ID
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00

7.5.21 Disable Module Site Command

The Disable Module Site command is used to disable a module site. If a module site is disabled, the IPMC firmware ignores the module inserted and acts as if the module is not present.

Table 7-51 Disable Module Site Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
	4	Module Site ID
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

7.5.22 Reset Carrier SDR Repository Command

The Reset Carrier SDR Repository command is used to clear and rebuild the carrier SDR repository.

Table 7-52 Reset Carrier SDR Repository Command Description

Type	Byte	Data Field
Request Data	1:3	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 1 = 0A, byte 2 = 40, byte 3 = 00
Response Data	1	Completion Code
	2:4	PPS IANA Private Enterprise ID 0x00400A = 16394 (Pigeon Point Systems) LSB Byte first: byte 2 = 0A, byte 3 = 40, byte 4 = 00

FRU Information and SDR Summary

8.1 Overview

This chapter provides the detailed description of default values of FRU information and sensor data records (SDRs) summary.

8.2 FRU Information

The blade provides the following FRU information in FRU ID 0.

Table 8-1 FRU information

Area	Description	Value	Access
Internal use area	Not used		
Board info area	Mfg date / time	According to Platform Management FRU information Storage Definition v1.0	r
	Board manufacturer	'EMERSON'	r
	Board product name	Product name of the specific blade variant	r
	Board serial number	Defined by manufacture	r
	Board part number	Product name of the specific blade variant	r
Product info area	Product manufacturer	'EMERSON'	r
	Product name	Product name of the specific blade variant	r
	Product serial number	Defined by manufacture	r
	Product part number	Product name of the specific blade variant	r

Table 8-1 FRU information (continued)

Area	Description	Value	Access
Multi record info area	Blade Point-To-Point Connectivity Record Area	PICMG record ID 0x14. The contents are described in the section 'E- Keying'.	r
	Carrier Information table record	PICMG record ID 0x1A.	r
	Carrier activation and current management record	PICMG record ID 0x17.	r
	Carrier point-to-point connectivity records	PICMG record ID 0x18.	r
	AMC point-to-point connectivity	PICMG record ID 0x19.	r
	SW and FW Version Information Record	OEM	r
	CPU Information Record	OEM	r

8.3 E-keying

The following table lists the e-keying information provided by the blade. The respective information is contained in the point-to-point connectivity record area.

The fiber channel interfaces (link type extension 2) described in the point-to-point connectivity record area are physically not supported by the blade.

Table 8-2 Contents of the Blade Point-to-Point Connectivity Record Area

No.	Link Grouping ID	Interface	Channel Number	Ports	Link Type	Link Type Extension
1	0	0 (Base Interface)	1	0 -SET 1 - NOT SET 2 - NOT SET 3 - NOT SET	0x01	0
2	0	0 (Base Interface)	2	0 -SET 1 - NOT SET 2 - NOT SET 3 - NOT SET	0x01	1
3	0	1 (Fabric Interface)	1	0 -SET 1 - SET 2 -SET 3 -SET	0x02	1
4	0	1 (Fabric Interface)	1	0 -SET 1 - NOT SET 2 - NOT SET 3 - NOT SET	0x02	0
5	0	1 (Fabric Interface)	2	0 -SET 1 - SET 2 -SET 3 -SET	0x02	1
6	0	1 (Fabric Interface)	2	0 -SET 1 - NOT SET 2 - NOT SET 3 - NOT SET	0x02	0

8.4 Power Configuration

The following table lists the power configuration of ATCA-7368 blade.

Table 8-3 Power Configuration

Item	Value	Description
Dynamic power reconfiguration support	No	While the blade is powered, it supports only power level
Dynamic power configuration	No	The power level is fixed and does not change
Number of power draw levels	1	The amount of possible power levels
Early Power Draw Levels, Watt	-	Complete early power level including IPMC

Table 8-3 Power Configuration (continued)

Item	Value	Description
Steady state power draw Levels, watt	Power Level 1: ATCA7368-0GB: 160W ATCA7368-0GB-LS: 165W ATCA7368-0GB-CE: 180W ATCA7368-0GB-LS-CE: 185W ATCA7368-0GB-LSL-CE: 185W	Complete steady power consumption including IPMC
Transition from early to steady levels, sec	0s	

8.5 Sensor Data Records

The following table lists the sensors available on the blades.

Table 8-4 Sensor Data Records

Sensor Name	Sensor Type	Sensor Number	Detailed SDR Description
HS Carrier	Hot Swap 0xF0	0x00	See Table 8-5 on page 154
HS AMC	Hot Swap 0xF0	0x01	See Table 8-6 on page 155
HS RTM	Hot Swap 0xF0	0x02	See Table 8-7 on page 156
-48V A Volts	Voltage 0x2	0x03	See Table 8-8 on page 157
-48V B Volts	Voltage 0x2	0x04	See Table 8-9 on page 158
-48V Amps	Current 0x3	0x05	See Table 8-10 on page 159
Holdup Cap Volts	Voltage 0x2	0x06	See Table 8-11 on page 161
Input Power	Other Unitsbased Sensor 0xb	0x07	See Table 8-12 on page 162

Table 8-4 Sensor Data Records (continued)

Sensor Name	Sensor Type	Sensor Number	Detailed SDR Description
PWR Status	OEM 0xD7	0x08	See Table 8-13 on page 163
Inlet Temp	Temperature 0x01	0x09	See Table 8-14 on page 164
Outlet Temp	Temperature 0x01	0x0A	See Table 8-15 on page 167
IPMC Temp	Temperature 0x01	0x0B	See Table 8-16 on page 170
CPU Temp	Temperature 0x01	0x0C	See Table 8-17 on page 171
DDR 1 Temp	Temperature 0x01	0x0D	See Table 8-18 on page 174
DDR 2 Temp	Temperature 0x01	0x0E	See Table 8-19 on page 175
DDR 3 Temp	Temperature 0x01	0x0F	See Table 8-20 on page 176
DDR 4 Temp	Temperature 0x01	0x10	See Table 8-21 on page 178
DDR 5 Temp	Temperature 0x01	0x11	See Table 8-22 on page 179
DDR 6 Temp	Temperature 0x01	0x12	See Table 8-23 on page 180
12.0V	Voltage 0x02	0x13	See Table 8-24 on page 182
3.3V	Voltage 0x02	0x14	See Table 8-25 on page 183
3.3V Mgmt	Voltage 0x02	0x15	See Table 8-26 on page 184
1.8V Eth	Voltage 0x02	0x16	See Table 8-27 on page 185
1.5V	Voltage 0x02	0x17	See Table 8-28 on page 187
1.2V	Voltage 0x02	0x18	See Table 8-29 on page 188
VCC CPU	Voltage 0x02	0x19	See Table 8-30 on page 189
1.5V DDR3	Voltage	0x1A	See Table 8-31 on page 191
IPMB0 Link	Physical IPMB-0 sensor 0xf1	0x1B	See Table 8-32 on page 192
BMC Watchdog	Watchdog 2 0x23	0x1C	See Table 8-33 on page 193
IPMC POST	Management Subsystem Health 0x28	0x1D	See Table 8-34 on page 194
Version Change	Version Change 0x2B	0x1E	See Table 8-35 on page 195

Table 8-4 Sensor Data Records (continued)

Sensor Name	Sensor Type	Sensor Number	Detailed SDR Description
FW Progress	System Firmware Progress 0x0F	0x1F	See Table 8-36 on page 196
OS Boot	OS boot 0x1F	0x20	See Table 8-37 on page 197
Boot Error	Boot Error 0x1E	0x21	See Table 8-38 on page 198
Boot Inited	System Boot Initiated 0x1D	0x22	See Table 8-39 on page 199
POST Code	OEM 0xD2	0x23	See Table 8-40 on page 200
IPMC Status	OEM 0xD5	0x24	See Table 8-41 on page 200
Power Good	Entity Presence 0x25	0x25	See Table 8-42 on page 201
Boot Bank	OEM 0xD2	0x26	See Table 8-43 on page 202
Reset Source	OEM 0xD2	0x27	See Table 8-44 on page 203
CPU Status	Processor 0x07	0x28	See Table 8-45 on page 204

The following figure shows the locations of all temperature sensors available on-board.

Figure 8-1 Location of Temperature Sensors

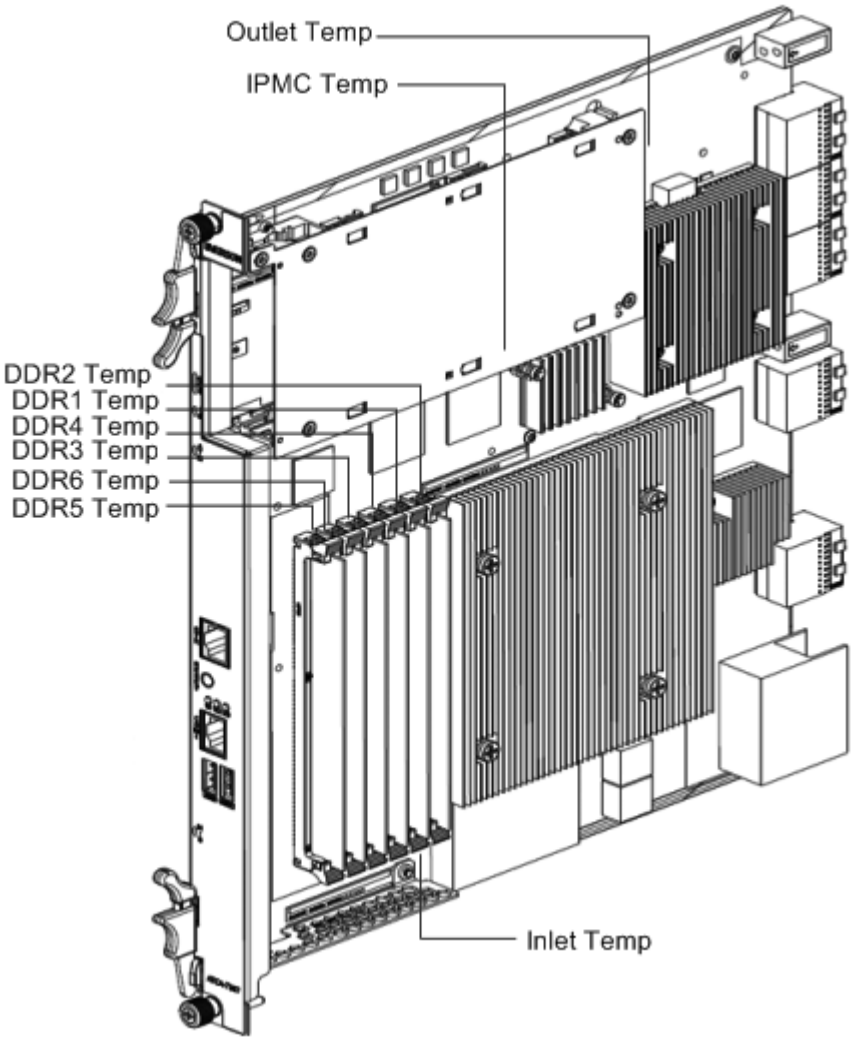


Table 8-5 HS Carrier

Feature	Raw Value	Description
Sensor Name	HS Carrier	-
Sensor LUN	0x00	-
Sensor Number	0x00	-
Entity ID	0xA0	PICMG Front Board
Sensor Type	0xF0	PICMG 3.0: FRU HotSwap
Event/Reading Type	0x6F	Discrete (sensor-specific)
Assertion Event Mask (Byte 15)	0xFF	-
Assertion Event Mask (Byte 16)	0x00	-
Deassertion Event Mask (Byte 17)	0x00	-
Deassertion Event Mask (Byte 18)	0x00	-
Threshold Mask (Byte 19)	0xFF	-
Threshold Mask (Byte 20)	0x00	-
Base Unit	0x00	(unspecified)
Rearm mode	0x01	Auto
Hysteresis Support	0x00	No Hysteresis or unspecified
Threshold Access Support	0x00	No Thresholds
Event Message Control	0x01	Entire Sensor only
Reading Definition	-	See PICMG 3.0 Specification,

Table 8-6 HS AMC

Feature	Raw Value	Description
Sensor Name	HS AMC	-
Sensor LUN	0x00	-
Sensor Number	0x01	-
Entity ID	0xC1	AMC module
Sensor Type	0xF0	ATCA hot swap
Event/Reading Type	0x6F	Sensor-specific
Assertion Event Mask (Byte 15)	0xFF	-
Assertion Event Mask (Byte 16)	0x00	-
Deassertion Event Mask (Byte 17)	0x00	-
Deassertion Event Mask (Byte 18)	0x00	-
Threshold Mask (Byte 19)	0xFF	-
Threshold Mask (Byte 20)	0x00	-
Base Unit	0x00	(unspecified)
Rearm mode	0x01	Auto
Hysteresis Support	0x00	No Hysteresis or unspecified
Threshold Access Support	0x00	No Thresholds
Event Message Control	0x01	Entire Sensor only
Reading Definition	-	-

Table 8-7 HS RTM

Feature	Raw Value	Description
Sensor Name	HS RTM	-
Sensor LUN	0x00	-
Sensor Number	0x02	-
Entity ID	0xC0	RTM module
Sensor Type	0xF0	ATCA hot swap
Event/Reading Type	0x6F	Sensor-specific
Assertion Event Mask (Byte 15)	0xFF	-
Assertion Event Mask (Byte 16)	0x00	-
Deassertion Event Mask (Byte 17)	0x00	-
Deassertion Event Mask (Byte 18)	0x00	-
Threshold Mask (Byte 19)	0xFF	-
Threshold Mask (Byte 20)	0x00	-
Base Unit	0x00	(unspecified)
Rearm mode	0x01	Auto
Hysteresis Support	0x00	No Hysteresis or unspecified
Threshold Access Support	0x00	No Thresholds
Event Message Control	0x01	Entire Sensor only
Reading Definition	-	-

Table 8-8 -48V A Volts

Feature	Raw Value	Description
Sensor Name	-48V A Volts	-
Sensor LUN	0x00	-
Sensor Number	0x03	-
Entity ID	0x0A	Power Supply
Sensor Type	0x02	Voltage
Event/Reading Type	0x01	Threshold
Assertion Event Mask (Byte 15)	0x14	-
Assertion Event Mask (Byte 16)	0x6A	-
Deassertion Event Mask (Byte 17)	0x14	-
Deassertion Event Mask (Byte 18)	0x6A	-
Threshold Mask (Byte 19)	0x36	-
Threshold Mask (Byte 20)	0x36	-
Base Unit	0x04	Volts
Rearm mode	0x01	Auto
Hysteresis Support	0x01	Readable
Threshold Access Support	0x02	Readable and settable
Event Message Control	0x00	Per Threshold/Discrete State
Nominal Reading	0x94	48
Upper non-recoverable threshold	0xE2	73.45
Upper critical threshold	0xDF	72.475

Table 8-8 -48V A Volts (continued)

Feature	Raw Value	Description
Upper non-critical threshold	0x00	(unspecified)
Lower non-recoverable threshold	0x74	37.7
Lower critical threshold	0x78	38.9
Lower non-critical threshold	0x00	(unspecified)
Reading Definition	Analog reading byte	Analog sensor reading

Table 8-9 -48V B Volts

Feature	Raw Value	Description
Sensor Name	-48V B Volts	-
Sensor LUN	0x00	-
Sensor Number	0x04	-
Entity ID	0x0A	Power Supply
Sensor Type	0x02	Voltage
Event/Reading Type	0x01	Threshold
Assertion Event Mask (Byte 15)	0x14	-
Assertion Event Mask (Byte 16)	0x6A	-
Deassertion Event Mask (Byte 17)	0x14	-
Deassertion Event Mask (Byte 18)	0x6A	-
Threshold Mask (Byte 19)	0x36	-
Threshold Mask (Byte 20)	0x36	-

Table 8-9 -48V B Volts (continued)

Feature	Raw Value	Description
Base Unit	0x04	Volts
Rearm mode	0x01	Auto
Hysteresis Support	0x01	Readable
Threshold Access Support	0x02	Readable and settable
Event Message Control	0x00	Per Threshold/Discrete State
Nominal Reading	0x94	48.1
Upper non-recoverable threshold	0xE2	73.45
Upper critical threshold	0xDF	72.475
Upper non-critical threshold	0x00	(unspecified)
Lower non-recoverable threshold	0x74	37.7
Lower critical threshold	0x78	38.9
Lower non-critical threshold	0x00	(unspecified)
Reading Definition	Analog reading byte	Analog sensor reading

Table 8-10 -48V Amps

Feature	Raw Value	Description
Sensor Name	-48V Current	-
Sensor LUN	0x00	-
Sensor Number	0x05	-
Entity ID	0x0A	Power Supply
Sensor Type	0x03	Current

Table 8-10 -48V Amps (continued)

Feature	Raw Value	Description
Event/Reading Type	0x01	Threshold
Assertion Event Mask (Byte 15)	0x80	
Assertion Event Mask (Byte 16)	0x0A	-
Deassertion Event Mask (Byte 17)	0x80	-
Deassertion Event Mask (Byte 18)	0x7A	-
Threshold Mask (Byte 19)	0x38	-
Threshold Mask (Byte 20)	0x38	-
Base Unit	0x05	Amps
Rearm mode	0x01	Auto
Hysteresis Support	0x01	Readable
Threshold Access Support	0x02	Readable and settable
Event Message Control	0x00	Per Threshold/Discrete State
Nominal Reading	0x36	5.076
Upper non-recoverable threshold	0x48	6.77
Upper critical threshold	0x45	6.49
Upper non-critical threshold	0x41	6.11
Lower non-recoverable threshold	0x00	(unspecified)
Lower critical threshold	0x00	(unspecified)
Lower non-critical threshold	0x00	(unspecified)
Reading Definition	Analog reading byte	Analog sensor reading

Table 8-11 Holdup Cap Volts

Feature	Raw Value	Description
Sensor Name	Holdup Cap Volts	-
Sensor LUN	0x00	-
Sensor Number	0x06	-
Entity ID	0x0A	Power Supply
Sensor Type	0x02	Voltage
Event/Reading Type	0x01	Threshold
Assertion Event Mask (Byte 15)	0x14	
Assertion Event Mask (Byte 16)	0x6A	-
Deassertion Event Mask (Byte 17)	0x14	-
Deassertion Event Mask (Byte 18)	0x6A	-
Threshold Mask (Byte 19)	0x36	-
Threshold Mask (Byte 20)	0x36	-
Base Unit	0x04	Volts
Rearm mode	0x01	Auto
Hysteresis Support	0x01	Readable
Threshold Access Support	0x02	Readable and settable
Event Message Control	0x00	Per Threshold/Discrete State
Nominal Reading	0xE4	90
Upper non-recoverable threshold	0xFF	101
Upper critical threshold	0xFA	99

Table 8-11 Holdup Cap Volts (continued)

Feature	Raw Value	Description
Upper non-critical threshold	0x00	(unspecified)
Lower non-recoverable threshold	0x60	38
Lower critical threshold	0x8B	55
Lower non-critical threshold	0x00	(unspecified)
Reading Definition	Analog reading byte	Analog sensor reading

Table 8-12 Input Power

Feature	Raw Value	Description
Sensor Name	Input Power	-
Sensor LUN	0x00	-
Sensor Number	0x07	-
Entity ID	0x0A	Power Supply
Sensor Type	0x0B	Other Units-based Sensor
Event/Reading Type	0x01	Threshold
Assertion Event Mask (Byte 15)	0x80	-
Assertion Event Mask (Byte 16)	0x0A	-
Deassertion Event Mask (Byte 17)	0x80	-
Deassertion Event Mask (Byte 18)	0x7A	-
Threshold Mask (Byte 19)	0x38	-
Threshold Mask (Byte 20)	0x38	-
Base Unit	0x04	Watts

Table 8-12 Input Power (continued)

Feature	Raw Value	Description
Rearm mode	0x01	Auto
Hysteresis Support	0x01	Readable
Threshold Access Support	0x02	Readable and settable
Event Message Control	0x00	Per Threshold/Discrete State
Nominal Reading	0x2A	50
Upper non-recoverable threshold	0xCE	250
Upper critical threshold	0xC6	241
Upper non-critical threshold	0xBD	230
Lower non-recoverable threshold	0x00	(unspecified)
Lower critical threshold	0x00	(unspecified)
Lower non-critical threshold	0x00	(unspecified)
Reading Definition	Analog reading byte	Analog sensor reading

Table 8-13 PWR Status

Feature	Raw Value	Description
Sensor Name	PWR Status	-
Sensor LUN	0x00	-
Sensor Number	0x08	-
Entity ID	0x0A	Power Supply
Sensor Type	0xD7	OEM Reserved
Event/Reading Type	0x6F	Discrete (sensor-specific)

Table 8-13 PWR Status (continued)

Feature	Raw Value	Description
Assertion Event Mask (Byte 15)	0xFF	-
Assertion Event Mask (Byte 16)	0x7F	-
Deassertion Event Mask (Byte 17)	0x00	-
Deassertion Event Mask (Byte 18)	0x00	-
Threshold Mask (Byte 19)	0xFF	-
Threshold Mask (Byte 20)	0x7F	-
Base Unit	0x00	(unspecified)
Rearm mode	0x01	Auto
Hysteresis Support	0x00	No Hysteresis or unspecified
Threshold Access Support	0x00	No Thresholds
Event Message Control	0x01	Entire Sensor only
Reading Definition	-	-

Table 8-14 Inlet Temp

Feature	Raw Value	Description
Sensor Name	Inlet Temp	-
Sensor LUN	0x00	-
Sensor Number	0x09	-
Entity ID	0xA0	PICMG Front Board
Sensor Type	0x01	Temperature
Event/Reading Type	0x01	Threshold

Table 8-14 Inlet Temp (continued)

Feature	Raw Value	Description
Assertion Event Mask (Byte 15)	0x80	-
Assertion Event Mask (Byte 16)	0x0A	-
Deassertion Event Mask (Byte 17)	0x80	-
Deassertion Event Mask (Byte 18)	0x7A	-
Threshold Mask (Byte 19)	0x38	-
Threshold Mask (Byte 20)	0x38	-
Base Unit	0x01	deg. C
Rearm mode	0x01	Auto
Hysteresis Support	0x02	Readable and Settable
Threshold Access Support	0x02	Readable and Settable
Event Message Control	0x00	Per Threshold/Discrete State
Nominal Reading	ATCA7368_0GB : 0x1F ATCA7368_0GB_LS : 0x1F ATCA7368_0GB_CE : 0x1E ATCA7368_0GB_L_CE : 0x1E ATCA7368_0GB_LS_CE : 0x1E ATCA7368_0GB_LSL_CE : 0x1E	ATCA7368_0GB : 31 ATCA7368_0GB_LS : 31 ATCA7368_0GB_CE : 30 ATCA7368_0GB_L_CE : 30 ATCA7368_0GB_LS_CE :30 ATCA7368_0GB_LSL_CE :30

Table 8-14 Inlet Temp (continued)

Feature	Raw Value	Description
Upper non-recoverable threshold	ATCA7368_0GB : 0x42 ATCA7368_0GB_LS : 0x42 ATCA7368_0GB_CE : 0x37 ATCA7368_0GB_L_CE : 0x37 ATCA7368_0GB_LS_CE : 0X37 ATCA7368_0GB_LSL_CE : 0X37	ATCA7368_0GB : 66 ATCA7368_0GB_LS : 66 ATCA7368_0GB_CE : 55 ATCA7368_0GB_L_CE : 55 ATCA7368_0GB_LS_CE : 55 ATCA7368_0GB_LSL_CE : 55
Upper critical threshold	ATCA7368_0GB : 0x39 ATCA7368_0GB_LS : 0x39 ATCA7368_0GB_CE : 0X2D ATCA7368_0GB_L_CE : 0X2D ATCA7368_0GB_LS_CE : 0x2D ATCA7368_0GB_LSL_CE : 0x2D	ATCA7368_0GB : 57 ATCA7368_0GB_LS : 57 ATCA7368_0GB_CE : 45 ATCA7368_0GB_L_CE : 45 ATCA7368_0GB_LS_CE : 45 ATCA7368_0GB_LSL_CE : 45
Upper non-critical threshold	ATCA7368_0GB : 0x2C ATCA7368_0GB_LS : 0x2C ATCA7368_0GB_CE : 0x23 ATCA7368_0GB_L_CE : 0x23 ATCA7368_0GB_LS_CE : 0x23 ATCA7368_0GB_LSL_CE : 0x23	ATCA7368_0GB : 44 ATCA7368_0GB_LS : 44 ATCA7368_0GB_CE : 35 ATCA7368_0GB_L_CE : 35 ATCA7368_0GB_LS_CE : 35 ATCA7368_0GB_LSL_CE : 35
Lower non-recoverable threshold	0x00	(unspecified)

Table 8-14 Inlet Temp (continued)

Feature	Raw Value	Description
Lower critical threshold	0x00	(unspecified)
Lower non-critical threshold	0x00	(unspecified)
Reading Definition	Analog reading byte	Analog sensor reading

Table 8-15 Outlet Temp

Feature	Raw Value	Description
Sensor Name	Outlet Temp	-
Sensor LUN	0x00	-
Sensor Number	0x0A	-
Entity ID	0xA0	PICMG Front Board
Sensor Type	0x01	Temperature
Event/Reading Type	0x01	Threshold
Assertion Event Mask (Byte 15)	0x80	-
Assertion Event Mask (Byte 16)	0x0A	-
Deassertion Event Mask (Byte 17)	0x80	-
Deassertion Event Mask (Byte 18)	0x7A	-
Threshold Mask (Byte 19)	0x38	-
Threshold Mask (Byte 20)	0x38	-
Base Unit	0x01	deg. C
Rearm mode	0x01	Auto
Hysteresis Support	0x02	Readable and settable

Table 8-15 Outlet Temp (continued)

Feature	Raw Value	Description
Threshold Access Support	0x02	Readable and settable
Event Message Control	0x00	Per Threshold/Discrete State
Nominal Reading	ATCA7368_0GB : 0x23 ATCA7368_0GB_LS : 0x23 ATCA7368_0GB_CE : 0x23 ATCA7368_0GB_L_CE : 0x23 ATCA7368_0GB_LS_CE : 0x23 ATCA7368_0GB_LSL_CE : 0x23	ATCA7368_0GB : 35 ATCA7368_0GB_LS : 35 ATCA7368_0GB_CE : 35 ATCA7368_0GB_L_CE : 35 ATCA7368_0GB_LS_CE :35 ATCA7368_0GB_LSL_CE :35
Upper non-recoverable threshold	ATCA7368_0GB : 0x50 ATCA7368_0GB_LS : 0x50 ATCA7368_0GB_CE : 0x46 ATCA7368_0GB_L_CE : 0x46 ATCA7368_0GB_LS_CE : 0x46 ATCA7368_0GB_LSL_CE : 0x46	ATCA7368_0GB : 80 ATCA7368_0GB_LS : 80 ATCA7368_0GB_CE : 70 ATCA7368_0GB_L_CE : 70 ATCA7368_0GB_LS_CE : 70 ATCA7368_0GB_LSL_CE : 70

Table 8-15 Outlet Temp (continued)

Feature	Raw Value	Description
Upper critical threshold	ATCA7368_0GB : 0x46 ATCA7368_0GB_LS : 0x46 ATCA7368_0GB_CE : 0x3c ATCA7368_0GB_L_CE : 0x3c ATCA7368_0GB_LS_CE : 0x3c ATCA7368_0GB_LSL_CE : 0x3c	ATCA7368_0GB : 70 ATCA7368_0GB_LS : 70 ATCA7368_0GB_CE : 60 ATCA7368_0GB_L_CE : 60 ATCA7368_0GB_LS_CE : 60 ATCA7368_0GB_LSL_CE : 60
Upper non-critical threshold	ATCA7368_0GB : 0x37 ATCA7368_0GB_LS : 0x37 ATCA7368_0GB_CE : 0x32 ATCA7368_0GB_L_CE : 0x32 ATCA7368_0GB_LS_CE : 0x32 ATCA7368_0GB_LSL_CE : 0x32	ATCA7368_0GB : 55 ATCA7368_0GB_LS : 55 ATCA7368_0GB_CE : 50 ATCA7368_0GB_L_CE : 50 ATCA7368_0GB_LS_CE : 50 ATCA7368_0GB_LSL_CE : 50
Lower non-recoverable threshold	0x00	(unspecified)
Lower critical threshold	0x00	(unspecified)
Lower non-critical threshold	0x00	(unspecified)
Reading Definition	Analog reading byte	Analog sensor reading

Table 8-16 IPMC Temp

Feature	Raw Value	Description
Sensor Name	IPMC Temp	-
Sensor LUN	0x00	-
Sensor Number	0x0B	-
Entity ID	0xA0	PICMG Front Board
Sensor Type	0x01	Temperature
Event/Reading Type	0x01	Threshold
Assertion Event Mask (Byte 15)	0x80	-
Assertion Event Mask (Byte 16)	0x0A	-
Deassertion Event Mask (Byte 17)	0x80	-
Deassertion Event Mask (Byte 18)	0x7A	-
Threshold Mask (Byte 19)	0x38	-
Threshold Mask (Byte 20)	0x38	-
Base Unit	0x01	deg. C
Rearm mode	0x01	Auto
Hysteresis Support	0x02	Readable and settable
Threshold Access Support	0x02	Readable and settable
Event Message Control	0x00	Per Threshold/Discrete State
Nominal Reading	0x25	37
Upper non-recoverable threshold	0x55	85
Upper critical threshold	0x4B	75

Table 8-16 IPMC Temp (continued)

Feature	Raw Value	Description
Upper non-critical threshold	0x41	65
Lower non-recoverable threshold	0x00	(unspecified)
Lower critical threshold	0x00	(unspecified)
Lower non-critical threshold	0x00	(unspecified)
Reading Definition	Analog reading byte	Analog sensor reading

Table 8-17 CPU Temp

Feature	Raw Value	Description
Sensor Name	CPU Temp	-
Sensor LUN	0x00	-
Sensor Number	0x0C	-
Entity ID	0xA0	PICMG Front Board
Sensor Type	0x01	Temperature
Event/Reading Type	0x01	Threshold
Assertion Event Mask (Byte 15)	0x80	-
Assertion Event Mask (Byte 16)	0x0A	-
Deassertion Event Mask (Byte 17)	0x80	-
Deassertion Event Mask (Byte 18)	0x0A	-
Threshold Mask (Byte 19)	0x38	-
Threshold Mask (Byte 20)	0x38	-
Base Unit	0x01	deg. C

Table 8-17 CPU Temp (continued)

Feature	Raw Value	Description
Rearm mode	0x01	Auto
Hysteresis Support	0x02	Readable and settable
Threshold Access Support	0x02	Readable and settable
Event Message Control	0x00	Per Threshold/Discrete State
Nominal Reading	ATCA7368_0GB : 0x32 ATCA7368_0GB_LS : 0x32 ATCA7368_0GB_CE : 0x32 ATCA7368_0GB_L_CE : 0x32 ATCA7368_0GB_LS_CE : 0x32 ATCA7368_0GB_LSL_CE : 0x32	ATCA7368_0GB : 50 ATCA7368_0GB_LS : 50 ATCA7368_0GB_CE : 50 ATCA7368_0GB_L_CE : 50 ATCA7368_0GB_LS_CE :50 ATCA7368_0GB_LSL_CE :50
Upper non-recoverable threshold	ATCA7368_0GB : 0x65 ATCA7368_0GB_LS : 0x65 ATCA7368_0GB_CE : 0x5E ATCA7368_0GB_L_CE : 0x5E ATCA7368_0GB_LS_CE : 0x5E ATCA7368_0GB_LSL_CE : 0x5E	ATCA7368_0GB : 101 ATCA7368_0GB-LS : 101 ATCA7368_0GB_CE : 94 ATCA7368_0GB_L_CE : 94 ATCA7368_0GB_LS_CE :94 ATCA7368_0GB_LSL_CE :94

Table 8-17 CPU Temp (continued)

Feature	Raw Value	Description
Upper critical threshold	ATCA7368_0GB : 0x5B ATCA7368_0GB_LS : 0x5B ATCA7368_0GB_CE : 0x54 ATCA7368_0GB_L_CE : 0x54 ATCA7368_0GB_LS_CE : 0x54 ATCA7368_0GB_LSL_CE : 0x54	ATCA7368_0GB : 91 ATCA7368_0GB_LS : 91 ATCA7368_0GB_CE :84 ATCA7368_0GB_L_CE :84 ATCA7368_0GB_LS_CE :84 ATCA7368_0GB_LSL_CE :84
Upper non-critical threshold	ATCA7368_0GB : 0x46 ATCA7368_0GB_LS : 0x46 ATCA7368_0GB_CE : 0x4A ATCA7368_0GB_L_CE : 0x4A ATCA7368_0GB_LS_CE : 0x4A ATCA7368_0GB_LSL_CE : 0x4A	ATCA7368_0GB : 70 ATCA7368_0GB_LS : 70 ATCA7368_0GB_CE : 74 ATCA7368_0GB_L_CE : 74 ATCA7368_0GB_LS_CE : 74 ATCA7368_0GB_LSL_CE : 74
Lower non-recoverable threshold	0x00	(unspecified)
Lower critical threshold	0x00	(unspecified)
Lower non-critical threshold	0x00	(unspecified)
Reading Definition	Analog reading byte	Analog sensor reading

Table 8-18 DDR 1 Temp

Feature	Raw Value	Description
Sensor Name	DDR 1 Temp	-
Sensor LUN	0x00	-
Sensor Number	0x0D	-
Entity ID	0xA0	PICMG Front Board
Sensor Type	0x01	Temperature
Event/Reading Type	0x01	Threshold
Assertion Event Mask (Byte 15)	0x80	-
Assertion Event Mask (Byte 16)	0x0A	-
Deassertion Event Mask (Byte 17)	0x80	-
Deassertion Event Mask (Byte 18)	0x0A	-
Threshold Mask (Byte 19)	0x38	-
Threshold Mask (Byte 20)	0x38	-
Base Unit	0x01	deg. C
Rearm mode	0x01	Auto
Hysteresis Support	0x02	Readable and settable
Threshold Access Support	0x02	Readable and settable
Event Message Control	0x00	Per Threshold/Discrete State
Nominal Reading	0x28	40
Upper non-recoverable threshold	0x5F	95
Upper critical threshold	0x55	85

Table 8-18 DDR 1 Temp (continued)

Feature	Raw Value	Description
Upper non-critical threshold	0x4B	75
Lower non-recoverable threshold	0x00	(unspecified)
Lower critical threshold	0x00	(unspecified)
Lower non-critical threshold	0x00	(unspecified)
Reading Definition	Analog reading byte	Analog sensor reading

Table 8-19 DDR 2 Temp

Feature	Raw Value	Description
Sensor Name	DDR 2 Temp	-
Sensor LUN	0x00	-
Sensor Number	0x0E	-
Entity ID	0xA0	PICMG Front Board
Sensor Type	0x01	Temperature
Event/Reading Type	0x01	Threshold
Assertion Event Mask (Byte 15)	0x80	-
Assertion Event Mask (Byte 16)	0x0A	-
Deassertion Event Mask (Byte 17)	0x80	-
Deassertion Event Mask (Byte 18)	0x0A	-
Threshold Mask (Byte 19)	0x38	-
Threshold Mask (Byte 20)	0x38	-
Base Unit	0x01	deg. C

Table 8-19 DDR 2 Temp (continued)

Feature	Raw Value	Description
Rearm mode	0x01	Auto
Hysteresis Support	0x02	Readable and settable
Threshold Access Support	0x02	Readable and settable
Event Message Control	0x00	Per Threshold/Discrete State
Nominal Reading	0x28	40
Upper non-recoverable threshold	0x5F	95
Upper critical threshold	0x55	85
Upper non-critical threshold	0x4B	75
Lower non-recoverable threshold	0x00	(unspecified)
Lower critical threshold	0x00	(unspecified)
Lower non-critical threshold	0x00	(unspecified)
Reading Definition	Analog reading byte	Analog sensor reading

Table 8-20 DDR 3 Temp

Feature	Raw Value	Description
Sensor Name	DDR 3 Temp	-
Sensor LUN	0x00	-
Sensor Number	0x0F	-
Entity ID	0xA0	PICMG Front Board
Sensor Type	0x01	Temperature
Event/Reading Type	0x01	Threshold

Table 8-20 DDR 3 Temp (continued)

Feature	Raw Value	Description
Assertion Event Mask (Byte 15)	0x80	-
Assertion Event Mask (Byte 16)	0x0A	-
Deassertion Event Mask (Byte 17)	0x80	-
Deassertion Event Mask (Byte 18)	0x0A	-
Threshold Mask (Byte 19)	0x38	-
Threshold Mask (Byte 20)	0x38	-
Base Unit	0x01	deg. C
Rearm mode	0x01	Auto
Hysteresis Support	0x02	Readable and settable
Threshold Access Support	0x02	Readable and settable
Event Message Control	0x00	Per Threshold/Discrete State
Nominal Reading	0x28	40
Upper non-recoverable threshold	0x5F	95
Upper critical threshold	0x55	85
Upper non-critical threshold	0x4B	75
Lower non-recoverable threshold	0x00	(unspecified)
Lower critical threshold	0x00	(unspecified)
Lower non-critical threshold	0x00	(unspecified)
Reading Definition	Analog reading byte	Analog sensor reading

Table 8-21 DDR 4 Temp

Feature	Raw Value	Description
Sensor Name	DDR 4 Temp	-
Sensor LUN	0x00	-
Sensor Number	0x10	-
Entity ID	0xA0	PICMG Front Board
Sensor Type	0x01	Temperature
Event/Reading Type	0x01	Threshold
Assertion Event Mask (Byte 15)	0x80	-
Assertion Event Mask (Byte 16)	0x0A	-
Deassertion Event Mask (Byte 17)	0x80	-
Deassertion Event Mask (Byte 18)	0x0A	-
Threshold Mask (Byte 19)	0x38	-
Threshold Mask (Byte 20)	0x38	-
Base Unit	0x01	deg. C
Rearm mode	0x01	Auto
Hysteresis Support	0x02	Readable and settable
Threshold Access Support	0x02	Readable and settable
Event Message Control	0x00	Per Threshold/Discrete State
Nominal Reading	0x28	40
Upper non-recoverable threshold	0x5F	95
Upper critical threshold	0x55	85

Table 8-21 DDR 4 Temp (continued)

Feature	Raw Value	Description
Upper non-critical threshold	0x4B	75
Lower non-recoverable threshold	0x00	(unspecified)
Lower critical threshold	0x00	(unspecified)
Lower non-critical threshold	0x00	(unspecified)
Reading Definition	Analog reading byte	Analog sensor reading

Table 8-22 DDR 5 Temp

Feature	Raw Value	Description
Sensor Name	DDR 5 Temp	-
Sensor LUN	0x00	-
Sensor Number	0x11	-
Entity ID	0xA0	PICMG Front Board
Sensor Type	0x01	Temperature
Event/Reading Type	0x01	Threshold
Assertion Event Mask (Byte 15)	0x80	-
Assertion Event Mask (Byte 16)	0x0A	-
Deassertion Event Mask (Byte 17)	0x80	-
Deassertion Event Mask (Byte 18)	0x0A	-
Threshold Mask (Byte 19)	0x38	-
Threshold Mask (Byte 20)	0x38	-
Base Unit	0x01	deg. C

Table 8-22 DDR 5 Temp (continued)

Feature	Raw Value	Description
Rearm mode	0x01	Auto
Hysteresis Support	0x02	Readable and settable
Threshold Access Support	0x02	Readable and settable
Event Message Control	0x00	Per Threshold/Discrete State
Nominal Reading	0x28	40
Upper non-recoverable threshold	0x5F	95
Upper critical threshold	0x55	85
Upper non-critical threshold	0x4B	75
Lower non-recoverable threshold	0x00	(unspecified)
Lower critical threshold	0x00	(unspecified)
Lower non-critical threshold	0x00	(unspecified)
Reading Definition	Analog reading byte	Analog sensor reading

Table 8-23 DDR 6 Temp

Feature	Raw Value	Description
Sensor Name	DDR 6 Temp	-
Sensor LUN	0x00	-
Sensor Number	0x12	-
Entity ID	0xA0	PICMG Front Board
Sensor Type	0x01	Temperature
Event/Reading Type	0x01	Threshold

Table 8-23 DDR 6 Temp (continued)

Feature	Raw Value	Description
Assertion Event Mask (Byte 15)	0x80	-
Assertion Event Mask (Byte 16)	0x0A	-
Deassertion Event Mask (Byte 17)	0x80	-
Deassertion Event Mask (Byte 18)	0x0A	-
Threshold Mask (Byte 19)	0x38	-
Threshold Mask (Byte 20)	0x38	-
Base Unit	0x01	deg. C
Rearm mode	0x01	Auto
Hysteresis Support	0x02	Readable and settable
Threshold Access Support	0x02	Readable and settable
Event Message Control	0x00	Per Threshold/Discrete State
Nominal Reading	0x28	40
Upper non-recoverable threshold	0x5F	95
Upper critical threshold	0x55	85
Upper non-critical threshold	0x4B	75
Lower non-recoverable threshold	0x00	(unspecified)
Lower critical threshold	0x00	(unspecified)
Lower non-critical threshold	0x00	(unspecified)
Reading Definition	Analog reading byte	Analog sensor reading

Table 8-24 12.0V

Feature	Raw Value	Description
Sensor Name	12.0V	-
Sensor LUN	0x00	-
Sensor Number	0x13	-
Entity ID	0x14	power module / DC-to-DC converter
Sensor Type	0x02	Voltage
Event/Reading Type	0x01	Threshold
Assertion Event Mask (Byte 15)	0x14	-
Assertion Event Mask (Byte 16)	0x6A	-
Deassertion Event Mask (Byte 17)	0x14	-
Deassertion Event Mask (Byte 18)	0x6A	-
Threshold Mask (Byte 19)	0x36	-
Threshold Mask (Byte 20)	0x36	-
Base Unit	0x04	Volts
Rearm mode	0x01	Auto
Hysteresis Support	0x02	Readable and settable
Threshold Access Support	0x02	Readable and settable
Event Message Control	0x00	Per Threshold/Discrete State
Nominal Reading	0xCE	12
Upper non-recoverable threshold	0xF0	13.9
Upper critical threshold	0xE5	13.3
Upper non-critical threshold	0x00	(unspecified)

Table 8-24 12.0V (continued)

Feature	Raw Value	Description
Lower non-recoverable threshold	0xAD	10.7
Lower critical threshold	0xB8	10.1
Lower non-critical threshold	0x00	(unspecified)
Reading Definition	Analog reading byte	Analog sensor reading

Table 8-25 3.3V

Feature	Raw Value	Description
Sensor Name	3.3V	-
Sensor LUN	0x00	-
Sensor Number	0x14	-
Entity ID	0x14	power module / DC-to-DC converter
Sensor Type	0x02	Voltage
Event/Reading Type	0x01	Threshold
Assertion Event Mask (Byte 15)	0x14	-
Assertion Event Mask (Byte 16)	0x6A	-
Deassertion Event Mask (Byte 17)	0x14	-
Deassertion Event Mask (Byte 18)	0x6A	-
Threshold Mask (Byte 19)	0x36	-
Threshold Mask (Byte 20)	0x36	-
Base Unit	0x04	Volts
Rearm mode	0x01	Auto
Hysteresis Support	0x02	Readable and settable

Table 8-25 3.3V (continued)

Feature	Raw Value	Description
Threshold Access Support	0x02	Readable and settable
Event Message Control	0x00	Per Threshold/Discrete State
Nominal Reading	0xAB	3.3
Upper non-recoverable threshold	0xBD	3.7
Upper critical threshold	0xB5	3.5
Upper non-critical threshold	0x00	(unspecified)
Lower non-recoverable threshold	0x98	3.1
Lower critical threshold	0xA0	2.9
Lower non-critical threshold	0x00	(unspecified)
Reading Definition	Analog reading byte	Analog sensor reading

Table 8-26 3.3V Mgmt

Feature	Raw Value	Description
Sensor Name	3.3V Mgmt	-
Sensor LUN	0x00	-
Sensor Number	0x15	-
Entity ID	0x14	power module / DC-to-DC converter
Sensor Type	0x02	Voltage
Event/Reading Type	0x01	Threshold
Assertion Event Mask (Byte 15)	0x14	-
Assertion Event Mask (Byte 16)	0x6A	-

Table 8-26 3.3V Mgmt (continued)

Feature	Raw Value	Description
Deassertion Event Mask (Byte 17)	0x14	-
Deassertion Event Mask (Byte 18)	0x6A	-
Threshold Mask (Byte 19)	0x36	-
Threshold Mask (Byte 20)	0x36	-
Base Unit	0x04	Volts
Rearm mode	0x01	Auto
Hysteresis Support	0x02	Readable and settable
Threshold Access Support	0x02	Readable and settable
Event Message Control	0x00	Per Threshold/Discrete State
Nominal Reading	0xAC	3.3
Upper non-recoverable threshold	0xBE	3.7
Upper critical threshold	0xB6	3.5
Upper non-critical threshold	0x00	(unspecified)
Lower non-recoverable threshold	0x99	3.1
Lower critical threshold	0xA1	2.9
Lower non-critical threshold	0x00	(unspecified)
Reading Definition	Analog reading byte	Analog sensor reading

Table 8-27 1.8V Eth

Feature	Raw Value	Description
Sensor Name	1.8V Eth	-
Sensor LUN	0x00	-

Table 8-27 1.8V Eth (continued)

Feature	Raw Value	Description
Sensor Number	0x16	-
Entity ID	0x14	power module / DC-to-DC converter
Sensor Type	0x02	Voltage
Event/Reading Type	0x01	Threshold
Assertion Event Mask (Byte 15)	0x14	-
Assertion Event Mask (Byte 16)	0x6A	-
Deassertion Event Mask (Byte 17)	0x14	-
Deassertion Event Mask (Byte 18)	0x6A	-
Threshold Mask (Byte 19)	0x36	-
Threshold Mask (Byte 20)	0x36	-
Base Unit	0x04	Volts
Rearm mode	0x01	Auto
Hysteresis Support	0x02	Readable and settable
Threshold Access Support	0x02	Readable and settable
Event Message Control	0x00	Per Threshold/Discrete State
Nominal Reading	0xB8	1.8
Upper non-recoverable threshold	0xCD	2.0
Upper critical threshold	0xC3	1.9
Upper non-critical threshold	0x00	(unspecified)
Lower non-recoverable threshold	0xA4	1.7
Lower critical threshold	0xAD	1.6

Table 8-27 1.8V Eth (continued)

Feature	Raw Value	Description
Lower non-critical threshold	0x00	(unspecified)
Reading Definition	Analog reading byte	Analog sensor reading

Table 8-28 1.5V

Feature	Raw Value	Description
Sensor Name	1.5V	-
Sensor LUN	0x00	-
Sensor Number	0x17	-
Entity ID	0x14	power module / DC-to-DC converter
Sensor Type	0x02	Voltage
Event/Reading Type	0x01	Threshold
Assertion Event Mask (Byte 15)	0x14	-
Assertion Event Mask (Byte 16)	0x6A	-
Deassertion Event Mask (Byte 17)	0x14	-
Deassertion Event Mask (Byte 18)	0x6A	-
Threshold Mask (Byte 19)	0x36	-
Threshold Mask (Byte 20)	0x36	-
Base Unit	0x04	Volts
Rearm mode	0x01	Auto
Hysteresis Support	0x02	Readable and settable
Threshold Access Support	0x02	Readable and settable
Event Message Control	0x00	Per Threshold/Discrete State

Table 8-28 1.5V (continued)

Feature	Raw Value	Description
Nominal Reading	0x9A	1.5
Upper non-recoverable threshold	0xAB	1.7
Upper critical threshold	0xA3	1.6
Upper non-critical threshold	0x00	(unspecified)
Lower non-recoverable threshold	0x89	1.4
Lower critical threshold	0x90	1.3
Lower non-critical threshold	0x00	(unspecified)
Reading Definition	Analog reading byte	Analog sensor reading

Table 8-29 1.2V

Feature	Raw Value	Description
Sensor Name	1.2V	-
Sensor LUN	0x00	-
Sensor Number	0x18	-
Entity ID	0x14	power module / DC-to-DC converter
Sensor Type	0x02	Voltage
Event/Reading Type	0x01	Threshold
Assertion Event Mask (Byte 15)	0x14	-
Assertion Event Mask (Byte 16)	0x6A	-
Deassertion Event Mask (Byte 17)	0x14	-
Deassertion Event Mask (Byte 18)	0x6A	-

Table 8-29 1.2V (continued)

Feature	Raw Value	Description
Threshold Mask (Byte 19)	0x36	-
Threshold Mask (Byte 20)	0x36	-
Base Unit	0x04	Volts
Rearm mode	0x01	Auto
Hysteresis Support	0x02	Readable and settable
Threshold Access Support	0x02	Readable and settable
Event Message Control	0x00	Per Threshold/Discrete State
Nominal Reading	0x7B	1.2
Upper non-recoverable threshold	0x88	1.4
Upper critical threshold	0x82	1.3
Upper non-critical threshold	0x00	(unspecified)
Lower non-recoverable threshold	0x6E	1.1
Lower critical threshold	0x74	1.0
Lower non-critical threshold	0x00	(unspecified)
Reading Definition	Analog reading byte	Analog sensor reading

Table 8-30 VCC CPU

Feature	Raw Value	Description
Sensor Name	VCC CPU	-
Sensor LUN	0x00	-
Sensor Number	0x19	-
Entity ID	0x14	power module / DC-to-DC converter

Table 8-30 VCC CPU (continued)

Feature	Raw Value	Description
Sensor Type	0x02	Voltage
Event/Reading Type	0x01	Threshold
Assertion Event Mask (Byte 15)	0x14	-
Assertion Event Mask (Byte 16)	0x6A	-
Deassertion Event Mask (Byte 17)	0x14	-
Deassertion Event Mask (Byte 18)	0x6A	-
Threshold Mask (Byte 19)	0x36	-
Threshold Mask (Byte 20)	0x36	-
Base Unit	0x04	Volts
Rearm mode	0x01	Auto
Hysteresis Support	0x02	Readable and settable
Threshold Access Support	0x02	Readable and settable
Event Message Control	0x00	Per Threshold/Discrete State
Nominal Reading	0x71	1.1
Upper non-recoverable threshold	0x98	1.49
Upper critical threshold	0x90	1.41
Upper non-critical threshold	0x00	(unspecified)
Lower non-recoverable threshold	0x4A	0.76
Lower critical threshold	0x4E	0.72
Lower non-critical threshold	0x00	(unspecified)
Reading Definition	Analog reading byte	Analog sensor reading

Table 8-31 1.5 DDR3

Feature	Raw Value	Description
Sensor Name	1.5 DDR3	-
Sensor LUN	0x00	-
Sensor Number	0x1A	-
Entity ID	0x14	power module / DC-to-DC converter
Sensor Type	0x02	Voltage
Event/Reading Type	0x01	Threshold
Assertion Event Mask (Byte 15)	0x14	-
Assertion Event Mask (Byte 16)	0x6A	-
Deassertion Event Mask (Byte 17)	0x14	-
Deassertion Event Mask (Byte 18)	0x6A	-
Threshold Mask (Byte 19)	0x36	-
Threshold Mask (Byte 20)	0x36	-
Base Unit	0x04	Volts
Rearm mode	0x01	Auto
Hysteresis Support	0x02	Readable and settable
Threshold Access Support	0x02	Readable and settable
Event Message Control	0x00	Per Threshold/Discrete State
Nominal Reading	0x9A	1.5
Upper non-recoverable threshold	0xA9	1.65
Upper critical threshold	0xA2	1.58

Table 8-31 1.5 DDR3 (continued)

Feature	Raw Value	Description
Upper non-critical threshold	0x00	(unspecified)
Lower non-recoverable threshold	0x7C	1.28
Lower critical threshold	0x83	1.21
Lower non-critical threshold	0x00	(unspecified)
Reading Definition	Analog reading byte	Analog sensor reading

Table 8-32 IPMB0 Link

Feature	Raw Value	Description
Sensor Name	IPMB0 Link	-
Sensor LUN	0x00	-
Sensor Number	0x1B	-
Entity ID	0xA0	PICMG Front Board
Sensor Type	0xF1	IPMB Status
Event/Reading Type	0x6F	Discrete (sensor-specific)
Assertion Event Mask (Byte 15)	0x0F	-
Assertion Event Mask (Byte 16)	0x00	-
Deassertion Event Mask (Byte 17)	0x00	-
Deassertion Event Mask (Byte 18)	0x00	-
Threshold Mask (Byte 19)	0x0F	-
Threshold Mask (Byte 20)	0x00	-
Base Unit	0x00	(unspecified)
Rearm mode	0x01	Auto

Table 8-32 IPMB0 Link (continued)

Feature	Raw Value	Description
Hysteresis Support	0x00	No Hysteresis or unspecified
Threshold Access Support	0x00	No Thresholds
Event Message Control	0x01	Entire Sensor only
Reading Definition	-	-

Table 8-33 BMC Watchdog

Feature	Raw Value	Description
Sensor Name	BMC Watchdog	-
Sensor LUN	0x00	-
Sensor Number	0x1C	-
Entity ID	0xA0	PICMG Front Board
Sensor Type	0x23	IPMI Watchdog Type 2
Event/Reading Type	0x6F	Discrete (sensor-specific)
Assertion Event Mask (Byte 15)	0x0F	-
Assertion Event Mask (Byte 16)	0x01	-
Deassertion Event Mask (Byte 17)	0x00	-
Deassertion Event Mask (Byte 18)	0x00	-
Threshold Mask (Byte 19)	0x0F	-
Threshold Mask (Byte 20)	0x01	-
Base Unit	0x00	(unspecified)
Rearm mode	0x01	Auto
Hysteresis Support	0x00	No Hysteresis or unspecified

Table 8-33 BMC Watchdog (continued)

Feature	Raw Value	Description
Threshold Access Support	0x00	No Thresholds
Event Message Control	0x01	Entire Sensor only
Reading Definition	-	-

Table 8-34 IPMC POST

Feature	Raw Value	Description
Sensor Name	IPMC POST	-
Sensor LUN	0x00	-
Sensor Number	0x1D	-
Entity ID	0x2E	Management Controller Firmware
Sensor Type	0x28	Management Subsystem Health
Event/Reading Type	0x6F	'digital' Discrete (generic)
Assertion Event Mask (Byte 15)	0x03	-
Assertion Event Mask (Byte 16)	0x00	-
Deassertion Event Mask (Byte 17)	0x00	-
Deassertion Event Mask (Byte 18)	0x00	-
Threshold Mask (Byte 19)	0x03	-
Threshold Mask (Byte 20)	0x00	-
Base Unit	0x00	(unspecified)
Rearm mode	0x01	Auto
Hysteresis Support	0x00	No Hysteresis or unspecified

Table 8-34 IPMC POST (continued)

Feature	Raw Value	Description
Threshold Access Support	0x00	No Thresholds
Event Message Control	0x01	Entire Sensor only
Reading Definition	-	-

Table 8-35 Version Change

Feature	Raw Value	Description
Sensor Name	Ver Change	-
Sensor LUN	0x00	-
Sensor Number	0x1E	-
Entity ID	0x2E	Management Controller Firmware
Sensor Type	0x2B	Version Change
Event/Reading Type	0x6F	Discrete (sensor-specific)
Assertion Event Mask (Byte 15)	0xFF	-
Assertion Event Mask (Byte 16)	0x00	-
Deassertion Event Mask (Byte 17)	0x00	-
Deassertion Event Mask (Byte 18)	0x00	-
Threshold Mask (Byte 19)	0xFF	-
Threshold Mask (Byte 20)	0x00	-
Base Unit	0x00	(unspecified)
Rearm mode	0x01	Auto
Hysteresis Support	0x00	No Hysteresis or unspecified
Threshold Access Support	0x00	No Thresholds

Table 8-35 Version Change (continued)

Feature	Raw Value	Description
Event Message Control	0x01	Entire Sensor only
Reading Definition	-	-

Table 8-36 FW Progress

Feature	Raw Value	Description
Sensor Name	FW Progress	-
Sensor LUN	0x00	-
Sensor Number	0x1F	-
Entity ID	0xA0	PICMG Front Board
Sensor Type	0x0F	IPMI System Firmware Progress
Event/Reading Type	0x6F	Sensor-specific
Assertion Event Mask (Byte 15)	0x07	-
Assertion Event Mask (Byte 16)	0x00	-
Deassertion Event Mask (Byte 17)	0x00	-
Deassertion Event Mask (Byte 18)	0x00	-
Threshold Mask (Byte 19)	0x07	-
Threshold Mask (Byte 20)	0x00	-
Base Unit	0x00	(unspecified)
Rearm mode	0x01	Auto
Hysteresis Support	0x00	No Hysteresis or unspecified
Threshold Access Support	0x00	No Thresholds
Event Message Control	0x01	Entire Sensor only

Table 8-36 FW Progress (continued)

Feature	Raw Value	Description
Reading Definition	-	-

Table 8-37 OS Boot

Feature	Raw Value	Description
Sensor Name	OS Boot	-
Sensor LUN	0x00	-
Sensor Number	0x20	-
Entity ID	0xA0	PICMG Front Board
Sensor Type	0x1F	OS boot
Event/Reading Type	0x6F	Sensor-specific
Assertion Event Mask (Byte 15)	0x7F	-
Assertion Event Mask (Byte 16)	0x00	-
Deassertion Event Mask (Byte 17)	0x00	-
Deassertion Event Mask (Byte 18)	0x00	-
Threshold Mask (Byte 19)	0x7F	-
Threshold Mask (Byte 20)	0x00	-
Base Unit	0x00	(unspecified)
Rearm mode	0x01	Auto
Hysteresis Support	0x00	No Hysteresis or unspecified
Threshold Access Support	0x00	No Thresholds
Event Message Control	0x01	Entire Sensor only
Reading Definition	-	See IPMI 1.5 Specification,

Table 8-37 OS Boot (continued)

Feature	Raw Value	Description
chapter "Sensor Type Codes and		
Data"		

Table 8-38 Boot Error

Feature	Raw Value	Description
Sensor Name	Boot Error	-
Sensor LUN	0x00	-
Sensor Number	0x21	-
Entity ID	0xA0	PICMG Front Board
Sensor Type	0x1E	Boot Error
Event/Reading Type	0x6F	Sensor-specific
Assertion Event Mask (Byte 15)	0x1F	-
Assertion Event Mask (Byte 16)	0x00	-
Deassertion Event Mask (Byte 17)	0x00	-
Deassertion Event Mask (Byte 18)	0x00	-
Threshold Mask (Byte 19)	0x1F	-
Threshold Mask (Byte 20)	0x00	-
Base Unit	0x00	(unspecified)
Rearm mode	0x01	Auto
Hysteresis Support	0x00	No Hysteresis or unspecified
Threshold Access Support	0x00	No Thresholds
Event Message Control	0x01	Entire Sensor only

Table 8-38 Boot Error (continued)

Feature	Raw Value	Description
Reading Definition	-	See IPMI 1.5 Specification,

Table 8-39 Boot Inited

Feature	Raw Value	Description
Sensor Name	Boot Inited	-
Sensor LUN	0x00	-
Sensor Number	0x22	-
Entity ID	0xA0	PICMG Front Board
Sensor Type	0x1D	Boot Initiated
Event/Reading Type	0x6F	Sensor-specific
Assertion Event Mask (Byte 15)	0x1F	-
Assertion Event Mask (Byte 16)	0x00	-
Deassertion Event Mask (Byte 17)	0x00	-
Deassertion Event Mask (Byte 18)	0x00	-
Threshold Mask (Byte 19)	0x1F	-
Threshold Mask (Byte 20)	0x00	-
Base Unit	0x00	(unspecified)
Rearm mode	0x01	Auto
Hysteresis Support	0x00	No Hysteresis or unspecified
Threshold Access Support	0x00	No Thresholds
Event Message Control	0x01	Entire Sensor only
Reading Definition	-	-

Table 8-40 POST Code

Feature	Raw Value	Description
Sensor Name	POST Code	-
Sensor LUN	0x00	-
Sensor Number	0x23	-
Entity ID	0xA0	PICMG Front Board
Sensor Type	0xD2	-
Event/Reading Type	0x6F	Sensor-specific
Assertion Event Mask (Byte 15)	0xFF	-
Assertion Event Mask (Byte 16)	0x00	-
Deassertion Event Mask (Byte 17)	0x00	-
Deassertion Event Mask (Byte 18)	0x00	-
Threshold Mask (Byte 19)	0xFF	-
Threshold Mask (Byte 20)	0x00	-
Base Unit	0x00	(unspecified)
Rearm mode	0x01	Auto
Hysteresis Support	0x00	No Hysteresis or unspecified
Threshold Access Support	0x00	No Thresholds
Event Message Control	0x01	Entire Sensor only
Reading Definition	-	-

Table 8-41 IPMC Status

Feature	Raw Value	Description
Sensor Name	IPMC Status	-
Sensor LUN	0x00	-

Table 8-41 IPMC Status (continued)

Feature	Raw Value	Description
Sensor Number	0x24	-
Entity ID	0xA0	PICMG Front Board
Sensor Type	0xD5	Artesyn IPMC Status
Event/Reading Type	0x6F	Sensor-specific
Assertion Event Mask (Byte 15)	0x00	-
Assertion Event Mask (Byte 16)	0x00	-
Deassertion Event Mask (Byte 17)	0x00	-
Deassertion Event Mask (Byte 18)	0x00	-
Threshold Mask (Byte 19)	0x7F	-
Threshold Mask (Byte 20)	0x00	-
Base Unit	0x00	(unspecified)
Rearm mode	0x01	Auto
Hysteresis Support	0x00	No Hysteresis or unspecified
Threshold Access Support	0x00	No Thresholds
Event Message Control	0x01	Entire Sensor only
Reading Definition	-	-

Table 8-42 Power Good

Feature	Raw Value	Description
Sensor Name	Power Good	-
Sensor LUN	0x00	-
Sensor Number	0x25	-

Table 8-42 Power Good (continued)

Feature	Raw Value	Description
Entity ID	0x14	power module / DC-to-DC converter
Sensor Type	0x08	Power supply
Event/Reading Type	0x6F	Sensor-specific
Assertion Event Mask (Byte 15)	0x03	-
Assertion Event Mask (Byte 16)	0x00	-
Deassertion Event Mask (Byte 17)	0x00	-
Deassertion Event Mask (Byte 18)	0x00	-
Threshold Mask (Byte 19)	0x03	-
Threshold Mask (Byte 20)	0x00	-
Base Unit	0x00	(unspecified)
Rearm mode	0x01	Auto
Hysteresis Support	0x00	No Hysteresis or unspecified
Threshold Access Support	0x00	No Thresholds
Event Message Control	0x01	Entire Sensor only
Reading Definition	-	-

Table 8-43 Boot Bank

Feature	Raw Value	Description
Sensor Name	Boot Bank	-
Sensor LUN	0x00	-
Sensor Number	0x26	-
Entity ID	0xA0	PICMG Front Board

Table 8-43 Boot Bank (continued)

Feature	Raw Value	Description
Sensor Type	0xD2	Artesyn OEM
Event/Reading Type	0x6F	Sensor-specific
Assertion Event Mask (Byte 15)	0x01	-
Assertion Event Mask (Byte 16)	0x00	-
Deassertion Event Mask (Byte 17)	0x00	-
Deassertion Event Mask (Byte 18)	0x00	-
Threshold Mask (Byte 19)	0x01	-
Threshold Mask (Byte 20)	0x00	-
Base Unit	0x00	(unspecified)
Rearm mode	0x01	Auto
Hysteresis Support	0x00	No Hysteresis or unspecified
Threshold Access Support	0x00	No Thresholds
Event Message Control	0x01	Entire Sensor only
Reading Definition	-	-

Table 8-44 Reset Source

Feature	Raw Value	Description
Sensor Name	Reset Source	-
Sensor LUN	0x00	-
Sensor Number	0x27	-
Entity ID	0xA0	PICMG Front Board
Sensor Type	0xD2	Artesyn-specific Discrete Digital

Table 8-44 Reset Source (continued)

Feature	Raw Value	Description
Event/Reading Type	0x6F	Sensor-specific
Assertion Event Mask (Byte 15)	0x7F	-
Assertion Event Mask (Byte 16)	0x00	-
Deassertion Event Mask (Byte 17)	0x00	-
Deassertion Event Mask (Byte 18)	0x00	-
Threshold Mask (Byte 19)	0x7F	-
Threshold Mask (Byte 20)	0x00	-
Base Unit	0x00	(unspecified)
Rearm mode	0x01	Auto
Hysteresis Support	0x00	No Hysteresis or unspecified
Threshold Access Support	0x00	No Thresholds
Event Message Control	0x01	Entire Sensor only
Reading Definition	-	-

Table 8-45 CPU Status

Feature	Raw Value	Description
Sensor Name	CPU Status	-
Sensor LUN	0x00	-
Sensor Number	0x28	-
Entity ID	0xA0	PICMG Front Board
Sensor Type	0x07	Processor
Event/Reading Type	0x6F	Sensor-specific

Table 8-45 CPU Status (continued)

Feature	Raw Value	Description
Assertion Event Mask (Byte 15)	0x02	-
Assertion Event Mask (Byte 16)	0x00	-
Deassertion Event Mask (Byte 17)	0x00	-
Deassertion Event Mask (Byte 18)	0x00	-
Threshold Mask (Byte 19)	0x02	-
Threshold Mask (Byte 20)	0x00	-
Base Unit	0x00	(unspecified)
Rearm mode	0x01	Auto
Hysteresis Support	0x00	No Hysteresis or unspecified
Threshold Access Support	0x00	No Thresholds
Event Message Control	0x01	Entire Sensor only
Reading Definition	-	-

The sensors available on the blades are listed in the following table.

For sensor threshold definition, use the "ipmitool" available at http://sourceforge.net/projects/ipmitool/files/ipmitool/ with the parameter "sensor".

Table 8-46 Sensor Data Records

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/Description	Assertion Deassertion	Rearm
0x00	HS Carrier	Hot Swap 0xF0	Sensor-specific discrete 0x6F	[7:4] = See IPMC Spec [3:0] = Current State (0, 1, 2, 3, 4, 5, 6 or 7)	[7:4] = Cause of State [3:0] = Previous State	[7:0] =FRU Device ID	For the Field: Current State/Previous State 0x0: M0 0x1: M1 0x2: M2 0x3: M3 0x4: M4 0x5: M5 0x6: M6 0x7: M7	Asrt	Auto
0x01	HS AMC	Hot Swap 0xF0	Sensor-specific discrete 0x6F	[7:4] = See IPMC Spec [3:0] = Current State (0, 1, 2, 3, 4, 5, 6 or 7)	[7:4] = Cause of state change [3:0] = Previous State	[7:0] =FRU Device ID	For the Field: Current State/Previous State 0x0: M0 0x1: M1 0x2: M2 0x3: M3 0x4: M4 0x5: M5 0x6: M6 0x7: M7	Asrt	Auto

Asrt: Assertion	Unr: Upper non-recoverable threshold	Uc: Upper critical threshold	Unc: Upper non-critical threshold
Deass: Deassertion	Lnr: Lower non-recoverable threshold	Lc: Lower critical threshold	Lnc: Lower non-critical threshold

Table 8-46 Sensor Data Records (continued)

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/Description	Assertion Deassertion	Rearm
0x02	HS RTM	Hot Swap 0xF0	Sensor-specific discrete 0x6F	[7:4] = See IPMC Spec [3:0] = Current State (0, 1, 2, 3, 4, 5, 6 or 7)	[7:4] = Cause of state change [3:0] = Previous State	[7:0] = FRU Device ID	For the Field: Current State/Previous State 0x0: M0 0x1: M1 0x2: M2 0x3: M3 0x4: M4 0x5: M5 0x6: M6 0x7: M7	Asrt	Auto
0x03	-48V A Volts	Voltage 0x02	Threshold 0x01	See IPMI Spec	reading	threshold	unr uc lnr lc	Asrt / Deass	Auto
0x04	-48V B Volts	Voltage 0x02	Threshold 0x01	See IPMI Spec	reading	threshold	unr uc lnr lc	Asrt/Deass	Auto
0x05	-48V Amps	Current 0x03	Threshold 0x01	See IPMI Spec	reading	threshold	unr uc unc	Asrt/Deass	Auto
0x06	HoldUp Cap Volts	Voltage 0x02	Threshold 0x01	See IPMI Spec	reading	threshold	unr uc lnr lc	Asrt/Deass	Auto
0x07	Input Power	Other Units-based Sensor 0xb	Threshold 0x01	See IPMI Spec	reading	threshold	unr uc unc	Asrt / Deass	Auto

Asrt: Assertion
Deass: Deassertion
Unr: Upper non-recoverable threshold
Lnr: Lower non-recoverable threshold
Uc: Upper critical threshold
Lc: Lower critical threshold
Unc: Upper non-critical threshold
Lnc: Lower non-critical threshold

Table 8-46 Sensor Data Records (continued)

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/Description	Assertion Deassertion	Rearm
0x08	PWR Status	OEM 0xD7	Sensor-specific discrete 0x6F	[7:4] = (See IPMC Spec) [3:0] = 0h	Synchor Pwr Entr Module: [6] = VOUT_low [5] = Hotswap [4] = Holdup [2] = Alarm [1] = Enable_B [0] Enable_A Emerson Pwr Entry Module: [7] = DIG_Fault [6] = HUCapEngage [5] = Hotswap_Enable [4] = HUCap_Switch [3] = Alarm_Control [1] = DIG_Alarm [0] = Sec_MCU_Fault All other bits are reserved	[7:6] = Pwr Entry Module 0 = Synchor 1 =Emerson Pwr Entry Module: All other bits are reserved	Pwr Entry Module Status Change detected	Asrt	Auto
0x09	Inlet Temp	Temperature 0x01	Threshold 0x01	See IPMI Spec	reading	threshold	unr uc unc	Asrt / Deass	Auto
0x0A	Outlet Temp	Temperature 0x01	Threshold 0x01	See IPMI Spec	reading	threshold	unr uc unc	Asrt / Deass	Auto
0x0B	IPMC temp	Temperature 0x01	Threshold 0x01	See IPMI Spec	reading	threshold	unr uc unc	Asrt / Deass	Auto
0x0C	CPU temp	Temperature 0x01	Threshold 0x01	See IPMI Spec	reading	threshold	unr uc unc	Asrt / Deass	Auto
0x0D	DDR 1 temp	Temperature 0x01	Threshold 0x01	See IPMI Spec	reading	threshold	unr uc unc	Asrt / Deass	Auto
0x0E	DDR 2 temp	Temperature 0x01	Threshold 0x01	See IPMI Spec	reading	threshold	unr uc unc	Asrt / Deass	Auto
0x0F	DDR 3 temp	Temperature 0x01	Threshold 0x01	See IPMI Spec	reading	threshold	unr uc unc	Asrt / Deass	Auto

Asrt: Assertion
Deass: Deassertion
Unr: Upper non-recoverable threshold
Lnr: Lower non-recoverable threshold
Uc: Upper critical threshold
Lc: Lower critical threshold
Unc: Upper non-critical threshold
Lnc: Lower non-critical threshold

Table 8-46 Sensor Data Records (continued)

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/Description	Assertion Deassertion	Rearm
0x10	DDR 4 temp	Temperature 0x01	Threshold 0x01	See IPMI Spec	reading	threshold	unr uc unc	Asrt / Deass	Auto
0x11	DDR 5 temp	Temperature 0x01	Threshold 0x01	See IPMI Spec	reading	threshold	unr uc unc	Asrt / Deass	Auto
0x12	DDR 6 temp	Temperature 0x01	Threshold 0x01	See IPMI Spec	reading	threshold	unr uc unc	Asrt / Deass	Auto
0x13	12.0V	Voltage 0x02	Threshold 0x01	See IPMI Spec	reading	threshold	unr uc lnr lc	Asrt / Deass	Auto
0x14	3.3V	Voltage 0x02	Threshold 0x01	See IPMI Spec	reading	threshold	unr uc lnr lc	Asrt / Deass	Auto
0x15	3.3V Mgmt	Voltage 0x02	Threshold 0x01	See IPMI Spec	reading	threshold	unr uc lnr lc	Asrt / Deass	Auto
0x16	1.8V Eth	Voltage 0x02	Threshold 0x01	See IPMI Spec	reading	threshold	unr uc lnr lc	Asrt / Deass	Auto
0x17	1.5V	Voltage 0x02	Threshold 0x01	See IPMI Spec	reading	threshold	unr uc lnr lc	Asrt / Deass	Auto
0x18	1.2V	Voltage 0x02	Threshold 0x01	See IPMI Spec	reading	threshold	unr uc lnr lc	Asrt / Deass	Auto
0x19	VCC CPU	Voltage 0x02	Threshold 0x01	See IPMI Spec	reading	threshold	unr uc lnr lc	Asrt / Deass	Auto
0x1A	1.5V DDR3	Voltage 0x02	ThreshHold 0X1	See IPMI Spec	reading	threshold	unr uc lnr lc	Asrt / Deass	Auto
0x1B	IPMB0 Link	physical IPMB-0 sensor 0xf1	Sensor-specific discrete 0x6F	[7:4] = (See IPMC Spec) [3:0] = Offset (0, 1, 2 or 3)	[7:4] = Channel Number. For AdvancedTCA®, this will typically be 0h to indicate IPMB-0 [3:0] = Reserved	reading (See PICMG 3.0 R3.0 Spec)	00h - IPMB-A disabled, IPMB-B disabled 01h - IPMB-A enabled, IPMB-B disabled 02h - IPMB-A disabled, IPMB-B enabled 03h - IPMB-A enabled, IPMP-B enabled	Asrt	Auto

Asrt: Assertion	Unr: Upper non-recoverable threshold	Uc: Upper critical threshold	Unc: Upper non-critical threshold
Deass: Deassertion	Lnr: Lower non-recoverable threshold	Lc: Lower critical threshold	Lnc: Lower non-critical threshold

Table 8-46 Sensor Data Records (continued)

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/Description	Assertion Deassertion	Rearm
0x1C	BMC Watchdog	Watchdog 2 0x23	Sensor-specific discrete 0x6F	[7:4] = (See IPMC Spec) [3:0] = Offset (0, 1, 2, 3 or 8)	See IPMI Spec	0xFF	0x0: Timer expired 0x1: Hard Reset 0x2: Power Down 0x3: Power Cycle 0x8: Timer Interrupt	Asrt	Auto
0x1D	IPMC POST	Management Subsystem Health 0x28	discrete 0x6	[7:4] = See IPMC Spec [3:0] = Offset (0, 1)	0xFF	0xFF	0x0: Performance Met 0x1: Performance Lags	Asrt	Auto
0x1E	Version Change	Version Change 0x2B	Sensor-specific discrete 0x6F	[7:4] = (See IPMC Spec) [3:0] = Offset (0, 1, 2, 3, 4, 5, 6, 7)	Change Type. (See IPMC Spec)	0xFF	0x0: Hardware change 0x1: Firmware or software change 0x2: Hardware incompatibility 0x3: Firmware or software incompatibility 0x4: Entity is of an invalid hardware version 0x5: Entity contains invalid F/W,software 0x6: Hardware Change successful 0x7: Software or F/W change successful	Asrt	Auto
0x1F	Fw Progress	System Firmware Progress 0x0F	Sensor-specific discrete 0x6F	[7:4] = (See IPMC Spec) [3:0] = Offset (1)	See IPMI Spec	See IPMI Spec	0x0: System Firmware Error 0x1: System Firmware Hang 0x2: System Firmware Progress	Asrt	Auto

Asrt: Assertion
Deass: Deassertion
Unr: Upper non-recoverable threshold
Lnr: Lower non-recoverable threshold
Uc: Upper critical threshold
Lc: Lower critical threshold
Unc: Upper non-critical threshold
Lnc: Lower non-critical threshold

Table 8-46 Sensor Data Records (continued)

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/Description	Assertion Deassertion	Rearm
0x20	OS Boot	OS Boot 0x1F	Sensor-specific discrete 0x6F				0x0: A: boot completed 0x1: C: boot completed 0x2: PXE boot completed 0x3: Diagnostic boot completed 0x4: CD_ROM boot completed 0x5: ROM boot completed 0x6: boot completed		Auto
0x21	Boot Error	Boot Error 0x1E	Sensor-specific discrete 0x6F				Reserved for future use. There is no event from this sensor now.	Asrt	Auto
0x22	Boot Inited	System Boot Initiated 0x1D	Sensor-specific discrete 0x6F				0x0: Initiated by power up 0x1: Initiated by hard reset 0x2: Initiated by warm reset 0x3: User requested PXE boot 0x4: Automatic boot to diagnostic	Asrt	Auto
0x23	POST Code	OEM 0xD2	Sensor-specific discrete 0x6F				No Event for this Sensor Reading Value accord with EFI BIOS port80 status code.		Auto

Asrt: Assertion
Deass: Deassertion
Unr: Upper non-recoverable threshold
Lnr: Lower non-recoverable threshold
Uc: Upper critical threshold
Lc: Lower critical threshold
Unc: Upper non-critical threshold
Lnc: Lower non-critical threshold

Table 8-46 Sensor Data Records (continued)

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/Description	Assertion Deassertion	Rearm
0x24	IPMC Status	OEM 0xD5	Sensor-specific discrete 0x6F				No Event for this sensor. Reading Value = 0; Present Status: [0:2] Reset Cause 0x1 = Watchdog Reset 0x2 = Software Reset 0x4 = Power on Reset [3:5] Reset Type 0x1 = Hard Boot 0x2 = Cold Boot 0x4 = Warm Boot [6:7] Reserved		Auto
0x25	Power Good	Entity Presence 0x25	Sensor-specific discrete 0x6F	[7:4] = (See IPMC Spec) [3:0] = Offset (0, 1)	0xFF	0xFF	0x0: Entity Present 0x1: Entity Absent	Asrt	Auto
0x26	Boot Bank	OEM 0xD2	Sensor-specific discrete 0x6F	0x0	0xFF	0xFF	Boot bank changed	Asrt	Auto

Asrt: Assertion
Deass: Deassertion
Unr: Upper non-recoverable threshold
Lnr: Lower non-recoverable threshold
Uc: Upper critical threshold
Lc: Lower critical threshold
Unc: Upper non-critical threshold
Lnc: Lower non-critical threshold

Table 8-46 Sensor Data Records (continued)

Sensor Number	Sensor Name	Sensor Type	Event/Reading Type	Event Data Byte 1	Event Data Byte 2	Event Data Byte 3	Event Threshold/Description	Assertion Deassertion	Rearm
0x27	Reset Source	OEM 0xD2	Sensor-specific discrete 0x6F	0xA0	bit0: RST_N: Payload Power-on reset bit1: Reserved bit2: FRB_PB_RST_N: Front board power button reset bit3: PLD_PL_RST_N: Payload Reset from PLD (IPMC) bit4: RTM_PB_RST_N: RTM power button reset bit5: WDG_RST_N: FPGA internal watchdog reset bit6: BIOS_RST_N: BIOS reset payload request bit7: OSYS_RST_N: OS reset payload 0: Reset not occurred 1: Reset occurred	[7:2] = Reserved [1] = IPMC Watchdog Timeout 0: No IPMC Watchdog Timeout 1: IPMC Watchdog Timeout occurred [0] = IPMC Watchdog Pre-Timeout 0: No IPMC Watchdog Pre-Timeout 1: IPMC Watchdog Pre-Timeout occurred	Payload Reset detected. Cause delivered in Event Byte 2 and Byte 3	Asrt	Auto
0x28	CPU Status	Processor 0x07	Sensor-specific discrete 0x6F	[7:4] = (See IPMC Spec) [3:0] = Offset (1)	0xFF	0xFF	0x1: Thermal Trip	Asrt	Auto

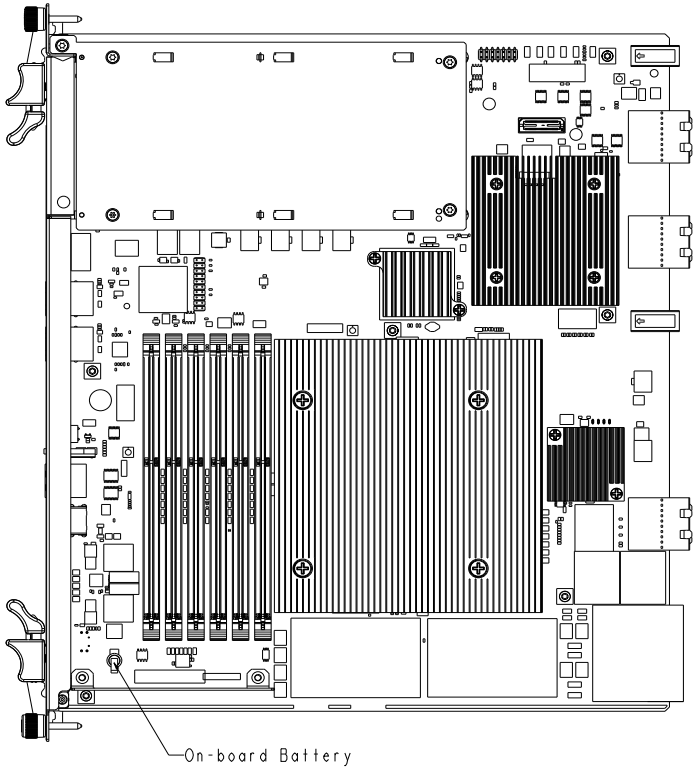
Asrt: Assertion
Deass: Deassertion
Unr: Upper non-recoverable threshold
Lnr: Lower non-recoverable threshold
Uc: Upper critical threshold
Lc: Lower critical threshold
Unc: Upper non-critical threshold
Lnc: Lower non-critical threshold

A.1 Replacing the Battery

Some blade variants contain an on-board battery. Its location is shown in the following figure.

A battery-less variant based on SUPERCAP is available on demand.

Figure A-1 Location of On-board Battery



The battery provides data retention of seven years summing up all periods of actual data use. Artesyn therefore assumes that there is usually no need to replace the battery except, for example, in case of long-term spare part handling.

NOTICE

Board/System Damage
Incorrect replacement of lithium batteries can result in a hazardous explosion.
Therefore, replace the battery as described in this chapter.

Data Loss
If the battery does not provide enough power anymore, the RTC is initialized and the data in the NVRAM is lost.
Therefore, replace the battery before seven years of actual battery use have elapsed.

Data Loss
Replacing the battery always results in data loss of the devices which use the battery as power backup.
Therefore, back up affected data before Replacing the battery.

Data Loss
If installing another battery type other than what is mounted at board delivery may cause data loss. Other battery types may be specified for other environments or may have a shorter lifespan.
Therefore, only use the same type of lithium battery as is already installed.

Replacement Procedure

To replace the battery, proceed as follows:

1. Remove battery.

NOTICE

PCB and Battery Holder Damage
Removing the battery with a screw driver may damage the PCB or the battery holder. To prevent this damage, do not use a screw driver to remove the battery from its holder.

2. Install the new battery following the "positive" and "negative" signs.

Related Documentation

B.1 Artesyn Embedded Technologies - Embedded Computing Documentation

The publications listed below are referenced in this manual. You can obtain electronic copies of Artesyn Embedded Technologies - Embedded Computing publications by contacting your local Artesyn sales office. For released products, you can also visit our Web site for the latest copies of our product documentation.

1. Go to www.artesyn.com/computing.
2. Under SUPPORT, click TECHNICAL DOCUMENTATION.
3. Under FILTER OPTIONS, click the Document types drop-down list box to select the type of document you are looking for.
4. In the Search text box, type the product name and click GO.

Table B-1 Artesyn Embedded Technologies - Embedded Computing Publications

Document Title	Publication Number
Basic Blade Services Software for the ATCA-7368 Programmer's Reference	6806800L95
ATCA-7368 Quick Start Guide	6806800N25
ATCA-7368 Safety Notes Summary	6806800N26

B.2 Related Specifications

For additional information, refer to the following table for related specifications. As an additional help, a source for the listed document is provided. Please note that, while these sources have been verified, the information is subject to change without notice.

Table B-2 Related Specifications

Organization	Document Title
PCI-SIG	PCI Local Bus Specification Revision 2.2 PCI-X Addendum to the PCI Local Bus Specification 1.0
PICMG	PICMG 3.0 Revision 2.0 Advanced TCA Base Specification PICMG 3.1 Revision 1.0 Specification Ethernet/Fiber Channel for AdvancedTCA Systems